BCM20203T512

Near Field Communication/13.56 MHz Radio Frequency Identification Read/Write IC

GENERAL DESCRIPTION

The BCM20203T512 has been developed to address Near Field Communication (NFC) and Radio Frequency Identification (RFID) tagging applications working to the ISO/IEC 18092, ISO/IEC 21481, and ISO/IEC 14443A standards.

The two-terminal BCM20203T512 IC, when connected to a loop antenna, produces a passive NFC/RFID tag operating in the standard unlicensed 13.56 MHz frequency band.

The read/write data in the BCM20203T512 memory is EEPROM-based, allowing for multiple read/write cycles. Individual blocks of memory can be locked into read-only operation by contactless command. Once selected, blocks or areas of memory are locked to be read-only; the process is irreversible.

The BCM20203T512 is based on a physical EEPROM array size of 512 bytes.

The BCM20203T512 gathers operational energy from the interrogation field generated by the NFC reader/writer unit, therefore, it operates passively, meaning that a battery is not required.

The BCM20203T512 can be supplied as die in the form of bumped, ground, and sawn wafers on film or as a 2.00 x 2.00 mm, 0.5 mm pitch, 6-lead DFN packaged IC.

FEATURES

- Compliant with the Type 1 tag format, which has been mandated by the NFC Forum
- Targeted for operation with NFC devices which work to ISO/IEC 18092 (NFCIP-1) and ISO/IEC 21481 (NFCIP-2)
- Designed to be compatible with the ISO/IEC 14443:2001, Parts 2 and 3
- ISO/IEC 14443 Type A modulation scheme
- Passive RFID tag operating in the unlicensed 13.56 MHz band
- Read and write (R/W) operation
- 8-byte read and 8-byte write commands
- Can be configured for One Time Programmable (OTP) and Write Once Read Many (WORM) operation
- Fast data communication rate of 106 kbps
- UID provision to enable collision detection by use of the Read UID (RID) command.
- Protection for data during the write operation by the BCM20203T512, only responding to commands prepended with a matching UID. Also provides protection in the situation where there are multiple tags present.
- Data communications are protected by 16-bit CRC integrity checking
- EEPROM based user read/write memory area organized as blocks of 8 bytes
- 7 bytes of Unique Identification (UID) number for use in data authentication/anticloning
- 480 bytes of user read/write memory
- 64 bits (8 bytes) of OTP memory
- All memory areas are individually one time lockable by RF command to prevent further modification of data and to produce read-only functionality

APPLICATIONS

- For use in NFC Forum Tags/Smartposter/Connection Handover/One-touch Setup (Simple Pairing) applications, as well as general 13.56 MHz RFID applications.

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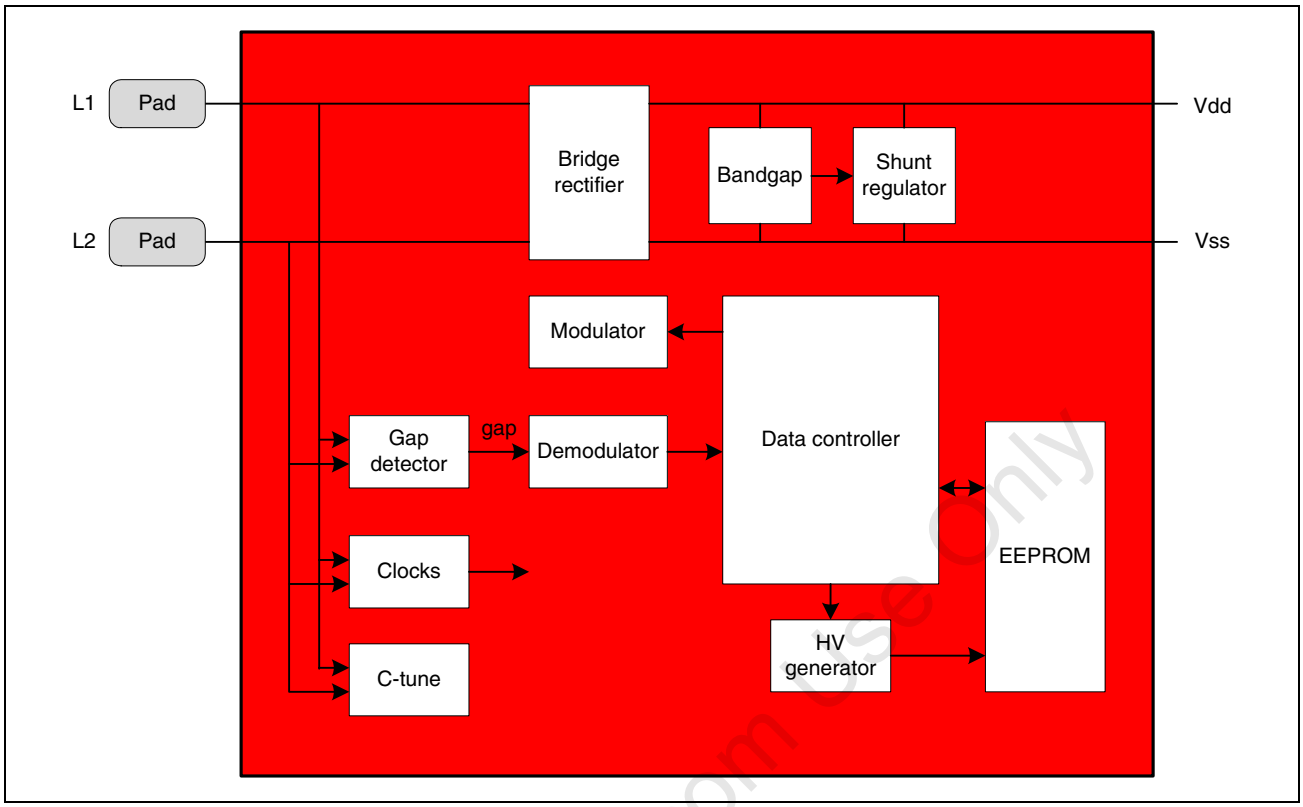

Figure 1: Outline Block Diagram

Revision History

Revision	*Date*	*Change Description*
20203T512-DS102-R	1/07/11	**Updated:** • "Description" on page 8 • "EEPROM Memory Map (Segment0)" on page 42
20203T512-DS101-R	11/30/10	**Updated:** • Table 21: "Ordering Information," on page 46 **Added:** • DFN package to General Description, page 1 • Figure 3: "Application Circuit for DFN Package as a Standalone Tag," on page 9 • Figure 4: "Application Circuit for DFN Package as a Tag with a Host Wake-up Interface," on page 10 • Section 7: "Mechanical Information," on page 45
20203T512-DS100-R	11/15/10	Initial release

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Section 1: Overview

Description

The BCM20203T512 has been developed to address Near Field Communication (NFC) and Radio Frequency Identification (RFID) tagging applications working to the ISO/IEC 18092, ISO/IEC 21481, and ISO/IEC 14443A standards.

The two-terminal BCM20203T512 IC, when connected to a loop antenna, produces a passive NFC/RFID tag operating in the standard unlicensed 13.56 MHz frequency band.

Sections in this document that discuss device functionality refer to the NFC/RFID tag as the BCM20203T512 tag, which is manufactured using the BCM20203T512 IC in conjunction with a suitable antenna. Sections that discuss the physical device refer to the BCM20203T512 die, wafer, or package.

The read/write data in the BCM20203T512 memory is EEPROM-based, allowing for multiple read/write cycles. Individual blocks of memory can be locked into read-only operation by contactless command. Once selected, blocks or areas of memory are locked to be read-only; the process is irreversible.

The BCM20203T512 gathers operational energy from the interrogation field generated by the NFC reader/ writer unit, therefore, it operates passively, meaning that a battery is not required.

See Figure 1 on page 2 for a block diagram of the BCM20203T512.

The BCM20203T512 is supplied pre-encoded in the NFC Forum defined Initialized state. This includes the capability container, memory layout TLVs, and empty NDEF message as defined in NFC Forum Type 1 Tag Operation Specification (see “NFC Forum ‘Initialized State’” on page 42).

Features

- For use in NFC Forum Tags/Smartposter/ Connection Handover/One-touch Setup applications as well as general 13.56 MHz RFID applications
- Targeted for operation with NFC devices which work to ISO/IEC 18092 (NFCIP-1) and ISO/IEC 21481 (NFCIP-2)
- Designed to be compatible with the ISO/IEC 14443:2001, Parts 2 and 3
- ISO/IEC 14443 Type A modulation scheme
- Passive RFID tag operating in the unlicensed 13.56 MHz band
- Read and write (R/W) operation
- 8-byte read (READ8) and 8-byte write (WRITE8) commands
- Can be configured for One Time Programmable (OTP) and Write Once Read Many (WORM) operation
- Fast data communication rate of 106 kbps
- UID provision to enable collision detection by use of the Read UID (RID) command.

- Protection for data during the write operation by the BCM20203T512, only responding to commands prepended with a matching UID. Also provides protection in the situation where there are multiple tags present.
- Fast byte write speed (options down to 1 ms)
- Data communications are protected by 16-bit CRC integrity checking
- EEPROM based user read/write memory area organized as blocks of 8 bytes
- 7 bytes of Unique Identification (UID) number for use in data authentication/anticloning
- 480 bytes of user read/write memory
- 64 bits (8 bytes) of OTP memory
- All memory areas are individually one time lockable by RF command to prevent further modification of data and to produce read-only functionality

Application Circuit

Figure 2 shows an application circuit for the BCM20203T512.

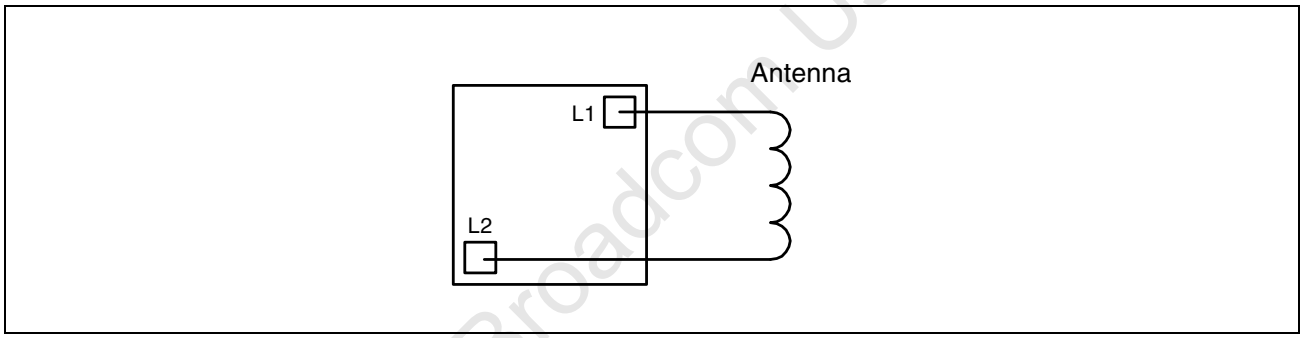


Figure 2: Application Circuit

Figure 3 shows an application circuit for the DFN package as a standalone tag.

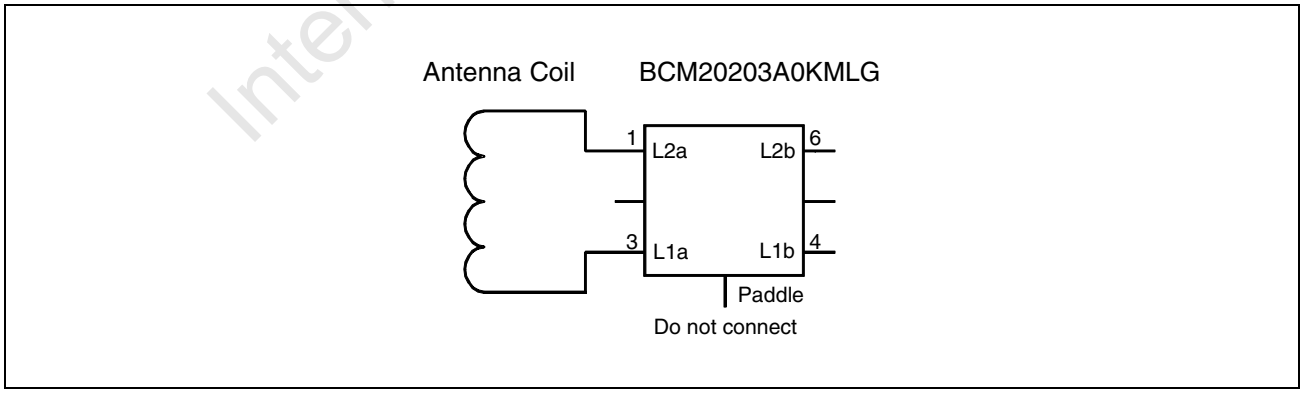


Figure 3: Application Circuit for DFN Package as a Standalone Tag

Note: Do not make any connection to the paddle shown in Figure 3, and more importantly, do not connect the paddle to ground.

Figure 4 shows an application circuit for the DFN package as a tag with a host wake-up interface.

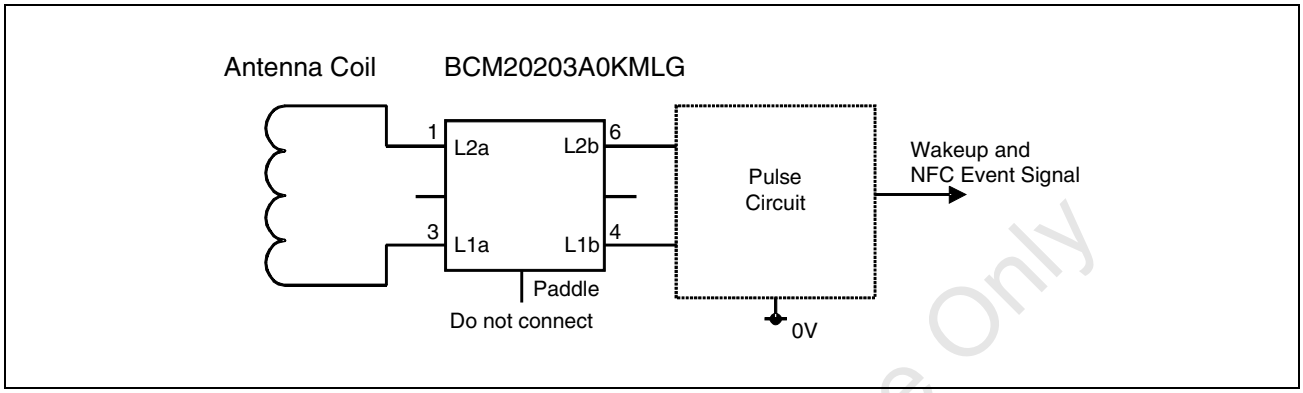


Figure 4: Application Circuit for DFN Package as a Tag with a Host Wake-up Interface

Note: Do not make any connection to the paddle shown in Figure 4, and more importantly, do not connect the paddle to ground.

Benefits

- Mandated as Type 1 Tag format by the NFC Forum for operation with NFC devices in reader/writer mode, hence, all future NFC Forum-compliant devices must operate with the BCM20203T512
- Initial Request-and-Answer communication cycle between the NFC reader/writer device and the BCM20203T512 follows the ISO/IEC 18092 and ISO/IEC 14443-3 standards
- Will operate with forthcoming ISO/IEC 18092 and ISO/IEC 21481-compliant NFC devices directly and with most existing ISO/IEC 14443 reader/writers after only software modification
- Fast read-all command (RALL) for 120-bytes
- Fast read segment command (RSEG) for each 128-byte segment of memory
- Time-efficient 8-byte read (READ8) and 8-byte write (WRITE8) commands
- High-integrity — 16-bit CRC protection on communications protocol
- Blocks of memory can be utilized as shadow areas for anti-tear protection measures
- Two bond pad die attachment
- Wire-bond, flip-chip, and module die attachment methods
- Suitable for operation with a wide variety of antenna coil sizes, form factors, and constructions

Memory Map

- 2 bytes of metal mask product identification header ROM
- 7 bytes of UID number
- 480 bytes of user read/write memory
- User read/write memory arranged as 60 blocks of 8 bytes
- Each 8-byte user read/write block is individually lockable by RFID command
- 64 bits (8 bytes) of One Time Programmable (OTP) bit area
- OTP bits can be set both individually or as multiple bits together in one command

Security

- 7-byte UID number is programmed and locked during manufacture
- Blocks can be programmed with application-specific data and then locked to provide read-only contents
- OTP bits can be used for non-reversible one-direction counters
- CRC protection on command and data communications to retain integrity
- All blocks, and hence all logical pages, have a one-time lock capability
- The BCM20203T512 can use a Digital Certificate or Seal based on the unalterable and unique identification number to authenticate and provide an appropriate level of security

General

- On-chip tuning capacitance designed for nominal 13.56 MHz operation
- Read range depends on the antenna used and reader specifications
- Fast write speed < 6.5 ms per byte as standard and per 8 bytes with WRITE-8 command
- Read Segment command for fast read access of each 128 byte segment of memory
- Data retention > 5 years
- Write operations > 10,000 cycles

C-tune

C-tune is the on-chip capacitance across the device pads L1 and L2 (expected use for tuning a coil connected across L1 and L2 to a frequency near to 13.56 MHz).

C-tune has been metal-mask selected as follows:

- C-tune standard = 21.1 pF, nominal

BCM20203T512 Identification

The BCM20203T512 contains a specific Header ROM value, fixed in memory area HR0, to identify that the tag is capable of carrying an NDEF Message as defined by the NFC Forum.

The header ROM, HR0 value is assigned as follows:

- BCM20203T96, HR0 = 11_h
- BCM20203T512, HR0 = 12_h

Qualification of the HR0 value must be used by a NFC reader/writer in order to identify and segregate between tags based on the BCM20203T96, the BCM20203T512, and other Broadcom ICs.

Section 2: Physical Memory Map

The 512-byte EEPROM array is arranged as 64 blocks of 8 bytes each. Each block is separately lockable.

There is an additional 2-byte Header ROM called HR0 and HR1, where HR0 = $1x_h$ identifies the tag as a Broadcom-family IC for NFC NDEF data applications. HR1 is reserved for internal use and should be ignored.

The contents are automatically included in the response packet to the Read ID (RID) and Read All (RALL) commands.

- HR0 = 12_h should be used to determine the BCM20203T512 with 512 byte memory map.
- HR1 = xx_h is undefined and should be ignored.

Table 1: EEPROM Memory Map (Segment0)

Type	*Block Number*	*Byte 0 (LSB)*	*Byte 1*	*Byte 2*	*Byte 3*	*Byte 4*	*Byte 5*	*Byte 6*	*Byte 7 (MSB)*	*Lockable*
UID	00	UID-0	UID-1	UID-2	UID-3	UID-4	UID-5	25_h[a]	Reserved	Locked
Data	01	Data0	Data1	Data2	Data3	Data4	Data5	Data6	Data7	Yes
Data	02	Data8	Data9	Data10	Data11	Data12	Data13	Data14	Data15	Yes
Data	03	Data16	Data17	Data18	Data19	Data20	Data21	Data22	Data23	Yes
Data	04	Data24	Data25	Data26	Data27	Data28	Data29	Data30	Data31	Yes
Data	05	Data32	Data33	Data34	Data35	Data36	Data37	Data38	Data39	Yes
Data	06	Data40	Data41	Data42	Data43	Data44	Data45	Data46	Data47	Yes
Data	07	Data48	Data49	Data50	Data51	Data52	Data53	Data54	Data55	Yes
Data	08	Data56	Data57	Data58	Data59	Data60	Data61	Data62	Data63	Yes
Data	09	Data64	Data65	Data66	Data67	Data68	Data69	Data70	Data71	Yes
Data	0A	Data72	Data73	Data74	Data75	Data76	Data77	Data78	Data79	Yes
Data	0B	Data80	Data81	Data82	Data83	Data84	Data85	Data86	Data87	Yes
Data	0C	Data88	Data89	Data90	Data91	Data92	Data93	Data94	Data95	Yes
Reserved	0D	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	N/A
Lock/OTP	0E	LOCK-0[b]	LOCK-1[b]	OTP-0[c]	OTP-1[c]	OTP-2[c]	OTP-3[c]	OTP-4[c]	OTP-5[c]	N/A
Lock/OTP	0F	OTP-6[c]	OTP-7[c]	LOCK-2[b]	LOCK-3[b]	LOCK-4[b]	LOCK-5[b]	LOCK-6[b]	LOCK-7[b]	N/A

Notes:

- Block 00: 7 bytes of Unique ID.
- Blocks 01–0C: All 96 data bytes are available to the user as read/write memory.
- Block 0D: Reserved for internal use.
- Block 0E: 2 bytes are used to store the individual block-lock status. 6 bytes are used for 48-OTP bits.
- Block 0F: 6 bytes are used to store the individual block-lock status. 2 bytes are used for 16-OTP bits.

a. This value in the UID is used to denote that the IC is a Broadcom part.
b. User block lock and status.
c. OTP bits.

Table 2: EEPROM Memory Map (Segment1)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	10	Data96	Data97	Data98	Data99	Data100	Data101	Data102	Data103	Yes
Data	11	Data104	Data105	Data106	Data107	Data108	Data109	Data110	Data111	Yes
Data	12	Data112	Data113	Data114	Data115	Data116	Data117	Data118	Data119	Yes
Data	13	Data120	Data121	Data122	Data123	Data124	Data125	Data126	Data127	Yes
Data	14	Data128	Data129	Data130	Data131	Data132	Data133	Data134	Data135	Yes
Data	15	Data136	Data137	Data138	Data139	Data140	Data141	Data142	Data143	Yes
Data	16	Data144	Data145	Data146	Data147	Data148	Data149	Data150	Data151	Yes
Data	17	Data152	Data153	Data154	Data155	Data156	Data157	Data158	Data159	Yes
Data	18	Data160	Data161	Data162	Data163	Data164	Data165	Data166	Data167	Yes
Data	19	Data168	Data169	Data170	Data171	Data172	Data173	Data174	Data175	Yes
Data	1A	Data176	Data177	Data178	Data179	Data180	Data181	Data182	Data183	Yes
Data	1B	Data184	Data185	Data186	Data187	Data188	Data189	Data190	Data191	Yes
Data	1C	Data192	Data193	Data194	Data195	Data196	Data197	Data198	Data199	Yes
Data	1D	Data200	Data201	Data202	Data203	Data204	Data205	Data206	Data207	Yes
Data	1E	Data208	Data209	Data210	Data211	Data212	Data213	Data214	Data215	Yes
Data	1F	Data216	Data217	Data218	Data219	Data220	Data221	Data222	Data223	Yes

Table 3: EEPROM Memory Map (Segment2)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	20	Data224	Data225	Data226	Data227	Data228	Data229	Data230	Data231	Yes
Data	21	Data232	Data233	Data234	Data235	Data236	Data237	Data238	Data239	Yes
Data	22	Data240	Data241	Data242	Data243	Data244	Data245	Data246	Data247	Yes
Data	23	Data248	Data249	Data250	Data251	Data252	Data253	Data254	Data255	Yes
Data	24	Data256	Data257	Data258	Data259	Data260	Data261	Data262	Data263	Yes
Data	25	Data264	Data265	Data266	Data267	Data268	Data269	Data270	Data271	Yes
Data	26	Data272	Data273	Data274	Data275	Data276	Data277	Data278	Data279	Yes
Data	27	Data280	Data281	Data282	Data283	Data284	Data285	Data286	Data287	Yes
Data	28	Data288	Data289	Data290	Data291	Data292	Data293	Data294	Data295	Yes
Data	29	Data296	Data297	Data298	Data299	Data300	Data301	Data302	Data303	Yes
Data	2A	Data304	Data305	Data306	Data307	Data308	Data309	Data310	Data311	Yes
Data	2B	Data312	Data313	Data314	Data315	Data316	Data317	Data318	Data319	Yes
Data	2C	Data320	Data321	Data322	Data323	Data324	Data325	Data326	Data327	Yes
Data	2D	Data328	Data329	Data330	Data331	Data332	Data333	Data334	Data335	Yes

Table 3: EEPROM Memory Map (Segment2)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	2E	Data336	Data337	Data338	Data339	Data340	Data341	Data342	Data343	Yes
Data	2F	Data344	Data345	Data346	Data347	Data348	Data349	Data350	Data351	Yes

Table 4: EEPROM Memory Map (Segment3)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	30	Data352	Data353	Data354	Data355	Data356	Data357	Data358	Data359	Yes
Data	31	Data360	Data361	Data362	Data363	Data364	Data365	Data366	Data367	Yes
Data	32	Data368	Data369	Data370	Data371	Data372	Data373	Data374	Data375	Yes
Data	33	Data376	Data377	Data378	Data379	Data380	Data381	Data382	Data383	Yes
Data	34	Data384	Data385	Data386	Data387	Data388	Data389	Data390	Data391	Yes
Data	35	Data392	Data393	Data394	Data395	Data396	Data397	Data398	Data399	Yes
Data	36	Data400	Data401	Data402	Data403	Data404	Data405	Data406	Data407	Yes
Data	37	Data408	Data409	Data410	Data411	Data412	Data413	Data414	Data415	Yes
Data	38	Data416	Data417	Data418	Data419	Data420	Data421	Data422	Data423	Yes
Data	39	Data424	Data425	Data426	Data427	Data428	Data429	Data430	Data431	Yes
Data	3A	Data432	Data433	Data434	Data435	Data436	Data437	Data438	Data439	Yes
Data	3B	Data440	Data441	Data442	Data443	Data444	Data445	Data446	Data447	Yes
Data	3C	Data448	Data449	Data450	Data451	Data452	Data453	Data454	Data455	Yes
Data	3D	Data456	Data457	Data458	Data459	Data460	Data461	Data462	Data463	Yes
Data	3E	Data464	Data465	Data466	Data467	Data468	Data469	Data470	Data471	Yes
Data	3F	Data472	Data473	Data474	Data475	Data476	Data477	Data478	Data479	Yes

Section 3: Device Operation

The RF interface of the BCM20203T512 tag is designed to be compliant with the type A variant in the ISO/IEC 14443-2:2001(E) standard.

The ISO/IEC 14443 terminology uses the term PCD for Proximity Coupling Device and PICC for Proximity Integrated Circuit(s) Card. This document uses the terms reader/writer for a PCD and the outlined BCM20203T512-based tag acting as a PICC.

The BCM20203T512 tag operates in accordance with ISO/IEC 14443A using the proprietary branch at Check ATQA (ISO/IEC 14443-3:2001(E) section 6.4.1).

A means of collision detection is provided so that the reader/writer knows if there is more than one tag in its field. This collision detection makes use of the 4 least significant bytes of the UID.

On power-up, the BCM20203T512 tag performs a power-on reset and remains 'silent' in Idle state until a REQA or WUPA command is received, upon which it moves to the Ready state as shown in Figure 5.

When in the Ready state, the BCM20203T512 tag waits for a proprietary command to move to the Execute state.

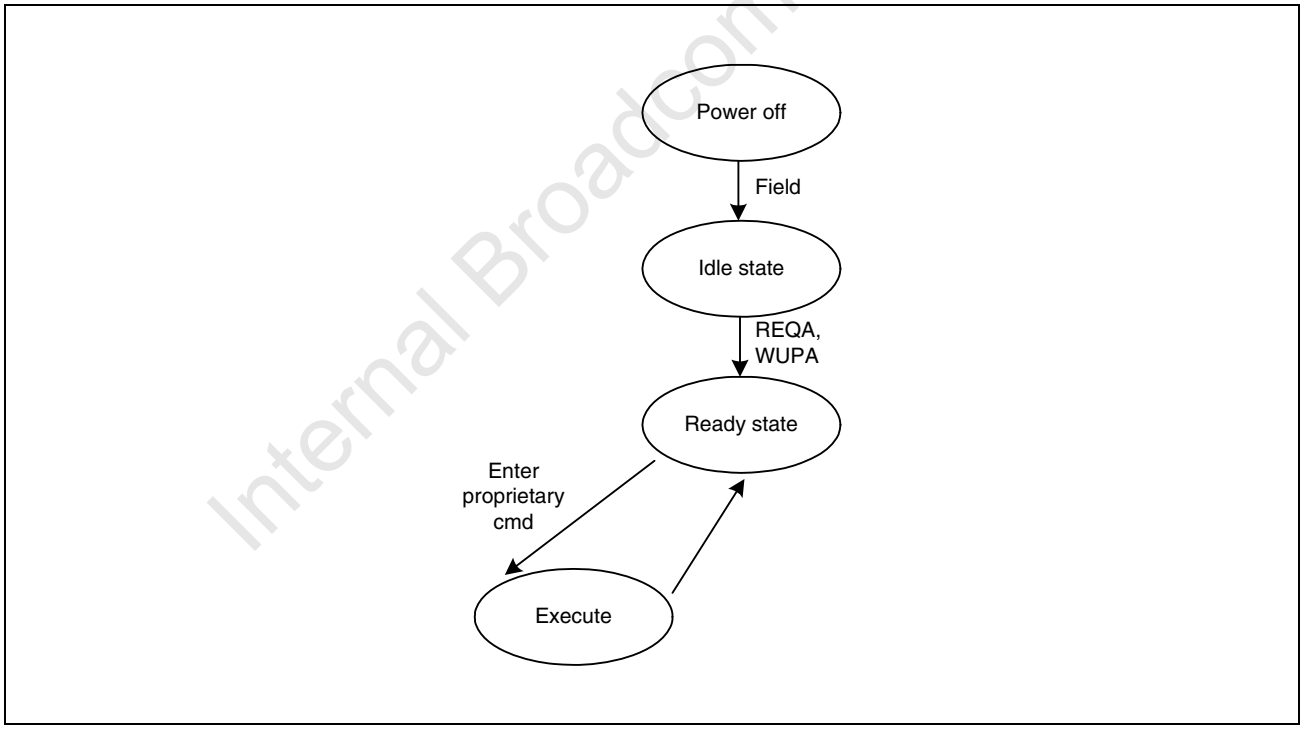


Figure 5: State Diagram

Section 4: Data Communication

Commands and Data to the BCM20203T512 Tag

Data communication or signalling to the BCM20203T512 tag is by means of 100% carrier modulation according to the type A variant in the ISO/IEC 14443-2:2001(E) and ISO/IEC 14443-3:2001(E) specifications.

Status and Data from the BCM20203T512 Tag

Data communication from the BCM20203T512 tag is achieved by modulation caused by varying the impedance of the tag as 'seen' by the coil of the reader/writer, according to the type A variant in the ISO/IEC 14443-2:2001(E) and ISO/IEC 14443-3:2001(E) specifications.

Frame Formats and Transmission Handling

Communication to the BCM20203T512 Tag

The communication from the reader/writer to the BCM20203T512 tag consists of a short frame containing the command byte followed by a series of zero or more proprietary frames.

Each seven- or eight-bit data set must be sent to the BCM20203T512 tag in a separate frame, therefore, a command sequence usually consists of several frames.

S = Start of frame

E = End of frame

After power-up, the BCM20203T512 tag only recognizes the **S** as a valid start-of-command sequence and a command will only be considered valid if there are 7 bits between **S** and **E**.

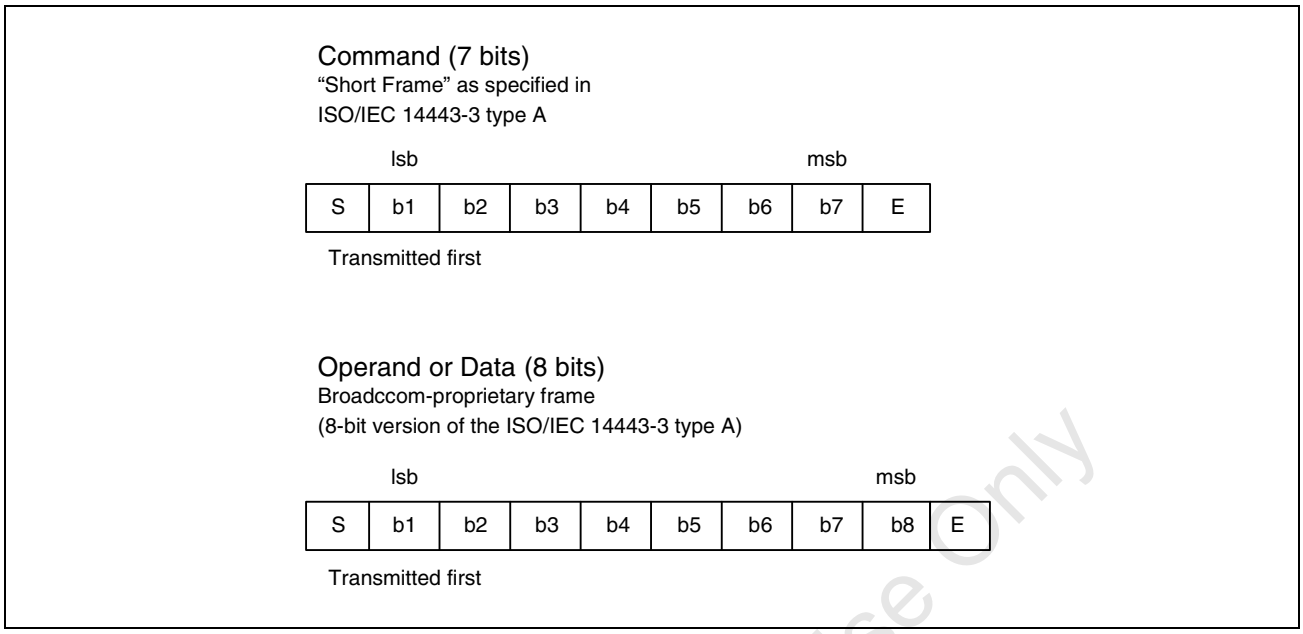


Figure 6: Frame Formats to the BCM20203T512 Tag

Communication from the BCM20203T512 Tag

Data output from the BCM20203T512 is sent as a single contiguous frame, as shown in Figure 7. The 8-bits of each data byte (together with each byte's parity bit) are concatenated into this single frame.

The overall frame format is the Standard Frame as specified for the type A variant in the ISO/IEC 14443-3:2001(E) standard [3].

S = Start-of-frame followed by one or more bytes (with the least significant bit first in each byte).

Each byte is followed by a P (parity bit) where the number of 1's is odd in (b1 to b8, P).

E = End-of-frame (after the last byte's parity bit).

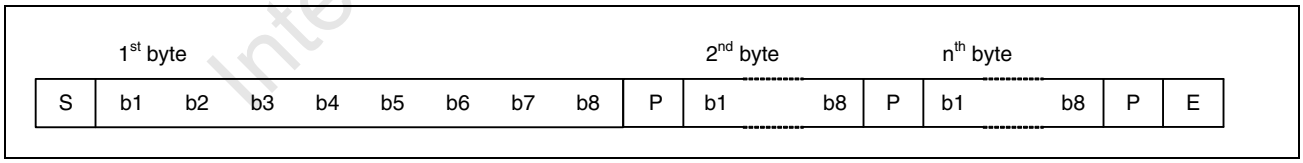


Figure 7: Frame Format from the BCM20203T512 Tag

Transmission Handling

The transmission between an NFC Device and the BCM20203T512 tag is half duplex and operates on the 'NFC Device talks first', command-response basis.

REQA and WUPA commands sent to a BCM20203T512 tag generate a 2-byte ATQA response according to the ISO/IEC 14443-3:2001(E) standard.

All other commands generate a response comprised of more than 2 bytes as shown in Table 5.

Table 5: Command-Response Byte Count

Command	*Command Bytes*	*Response Bytes*	*Applicable Memory Area*
REQA	1	2	N/A
WUPA	1	2	N/A
RID	9	8	HR0, HR1 and Block 0, bytes 0-3
RALL	9	124	HR0, HR1 and Blocks 0-E
READ	9	4	Blocks 0-E
WRITE-E	9	4	Blocks 0-E
WRITE-NE	9	4	Blocks 0-E
RSEG	16	131	Segments 0-3
READ8	16	11	Blocks 0-3F
WRITE-E8	16	11	Blocks 0-3F
WRITE-NE8	16	11	Blocks 0-3F

Table 6 and Table 7 show details of the sequence of Command and Response bytes for the BCM20203T512 based tag. With the exception of the REQA, WUPA, and ATQA, a 2-byte CRC must be appended to the end of all commands and responses as shown.

Table 6: Command-Response Summary

Command									***Response***									
REQA	–	–	–	–	–	–	–	–	ATQA0	ATQA1	–	–	–	–	–	–	–	–
WUPA	–	–	–	–	–	–	–	–	ATQA0	ATQA1	–	–	–	–	–	–	–	–
RID	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	CRC1	CRC2	HR0	HR1	UID0	UID1	UID2	UID3	CRC1	CRC2	–	–
RALL	00h[a]	00h[a]	UID0	UID1	UID2	UID3	CRC1	CRC2	HR0	HR1	UID0	UID1	….	….	….	Block-E Byte-7	CRC1	CRC2
READ	ADD	00h[a]	UID0	UID1	UID2	UID3	CRC1	CRC2	ADD	DAT	CRC1	CRC2	–	–	–	–	–	–
WRITE-E	ADD	DAT	UID0	UID1	UID2	UID3	CRC1	CRC2	ADD	DAT	CRC1	CRC2	–	–	–	–	–	–
WRITE-NE	ADD	DAT	UID0	UID1	UID2	UID3	CRC1	CRC2	ADD	DAT	CRC1	CRC2	–	–	–	–	–	–

a. Dummy frames.

Table 7: Command-Response Summary — Command

Command															
RSEG	ADDS	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	UID0	UID1	UID2	UID3	CRC1	CRC2
READ8	ADD8	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	00h[a]	UID0	UID1	UID2	UID3	CRC1	CRC2
WRITE-E8	ADD8	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	UID0	UID1	UID2	UID3	CRC1	CRC2
WRITE-NE8	ADD8	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	UID0	UID1	UID2	UID3	CRC1	CRC2

a. Dummy frames.

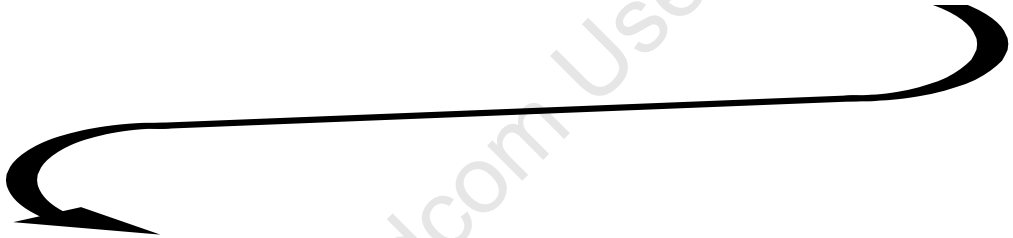


Table 8: Command-Response Summary — Response

Response												
ADDS	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	….	DAT127	CRC1	CRC2
ADD8	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	CRC1	CRC2	–	–
ADD8	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	CRC1	CRC2	–	–
ADD8	DAT0	DAT1	DAT2	DAT3	DAT4	DAT5	DAT6	DAT7	CRC1	CRC2	–	–

Section 5: Commands and Timing

Command Format

Table 9: List of Commands

Command	*Page*	*Command Code (7-bits)*							*Comment*
		msb						lsb	
		b7	b6	b5	b4	b3	b2	b1	
REQA	page 26	26h	0	1	0	0	1	1	0	Request Command, type A
WUPA	page 26	52_h	1	0	1	0	0	1	0	Wake-up, type A
RID	page 27	78_h	1	1	1	1	0	0	0	Read ID: Use to read the metal-mask ROM and UID0-3 from block 0
RALL	page 28	00_h	0	0	0	0	0	0	0	Read all (only blocks 0-E covered)
READ	page 29	01_h	0	0	0	0	0	0	1	Read (a single byte)
WRITE-E	page 30	53_h	1	0	1	0	0	1	1	Write-with-erase (a single byte)
WRITE-NE	page 31	$1A_h$	0	0	1	1	0	1	0	Write-no-erase (a single byte)
RSEG	page 32	10_h	0	0	1	0	0	0	0	Read segment
READ8	page 32	02_h	0	0	0	0	0	1	0	Read (8 bytes)
WRITE-E8	page 33	54_h	1	0	1	0	1	0	0	Write-with-erase (8 bytes)
WRITE-NE8	page 33	$1B_h$	0	0	1	1	0	1	1	Write-no-erase (8 bytes)

Address Operands

ADD

The format of the ADD address operand for the READ, WRITE-E, and WRITE-NE commands is shown in Table 10.

Block = select one of blocks 0_h – F_h

Byte = select one of bytes 0 – 7

Table 10: Format of Address Operand ADD

msb							lsb
b8	b7	b6	b5	b4	b3	b2	b1
0_b	Block				Byte		

ADDS

The format of the ADDS address operand for the RSEG command is shown in Table 11.

Segment = select one of the Segments 0_h – 3_h

Table 11: Format of Address Operand ADDS

msb							lsb
b8	b7	b6	b5	b4	b3	b2	b1
0_b	0_b	Segment		0_b	0_b	0_b	0_b

ADD8

The format of the ADD8 block address operand for the READ8, WRITE-E8, and WRITE-NE8 commands is shown in Table 12.

Block = select one of the 8-byte blocks 00_h – $3F_h$

Table 12: Format of Address Operand ADD8

msb							lsb
b8	b7	b6	b5	b4	b3	b2	b1
0_b	0_b	Global Block					

CRC

Except for the REQA and WUPA command, a 2-byte CRC must be included in each part of the command and response sequence. If the CRC value received by the tag does not match the one it internally generates as data arrives, then the BCM20203T512 tag will halt the operation and move to the READY state, waiting for the next command.

The CRC is the 16-bit version as specified under CRC-CCITT (see ISO/IEC 14443-3:2001(E) Annex B: CRC_B).

The CRC must be calculated on all data bits, including the header bytes, HR0 and HR1, however, start, end, parity (and the CRC bits themselves), are not included within the CRC calculation.

UID Echo

The reader/writer must provide a single tag selection feature by including the lower 4 bytes of UID as part of all the proprietary read and write commands. If the 4 lower bytes of UID do not match, then the BCM20203T512 tag will halt operation and remain in the Ready state, waiting for the next valid command.

Detailed Timing

From ISO/IEC 14443-3:2001(E), the command timing of a single-bit period shall nominally be defined using B = 9.4 µs, as follows.

(i) Frames to the BCM20203T512 tag: S = 1B; data = 8B; E = 2B

(ii) Frame from the BCM20203T512 tag: S=1B; E = 2B; data = 9B per byte

Table 13: Timing and Description Definitions

Name	*Description*	*Specification*
RRDD	Reader-Reader Data Delay The time between the end of the last pause of a frame transmitted by the reader/writer and the first pause of the next frame to be transmitted by the reader/writer.	Minimum: ≥ 28 µs when last bit was 1 ≥ 23 µs when last bit was 0 Maximum: None
DRD	BCM20203T512 Device Response Delay (Frame Delay Time) The time between the end of the last pause transmitted by the reader/writer and the first modulation edge within the start bit transmitted by the BCM20203T512 tag.[a]	FDT timing from ISO/IEC 14443-3:2001(E), section 6.1.2 where n: For REQA, WUPA, RID, READ, RALL, RSEG, READ: n=9 For WRITE-E, WRITE-E8: n=554 For WRITE-NE, WRITE-NE8: n=281 With tolerance for digital and analog elements of ± 6.5 clock cycles (13.56 MHz).
RRD	Reader Response Delay Delay time from BCM20203T512 tag to the reader/writer, i.e., the time between the last modulation transmitted by the BCM20203T512 tag and the first gap transmitted by the reader/writer.	ISO/IEC 14443-3:2001(E), section 6.1.3 1172/ fc ≅ 86 µs
CE	Command End	
UID-echo	The four least significant UID bytes from block 0 (LSB first)	

a. FDT definition in ISO/IEC 14443-3:2001(E), SECTION 6.1.2.

Table 14: FDT Timing Calculations

Command	*n*	*FDT_{bit-1} = 128n + 84*	*FDT_{bit-0} = 128n + 20*
REQA, WUPA, RID, READ, RALL, RSEG, READ8	9	1236/fc ≈ 91 µs	1172/fc ≈ 86 µs
WRITE-E, WRITE-E8	554	70996/fc ≈ 5236 µs	70932/fc ≈ 5231 µs
WRITE-NE, WRITE-NE8	281	36052/fc ≈ 2659 µs	35988/fc ≈ 2654 µs

REQA/WUPA Command

Note: Figure 8 on page 26 through Figure 13 on page 31 do not show lead-in, start, and end-of-frame bits, etc.

CE = Command End = Ready state

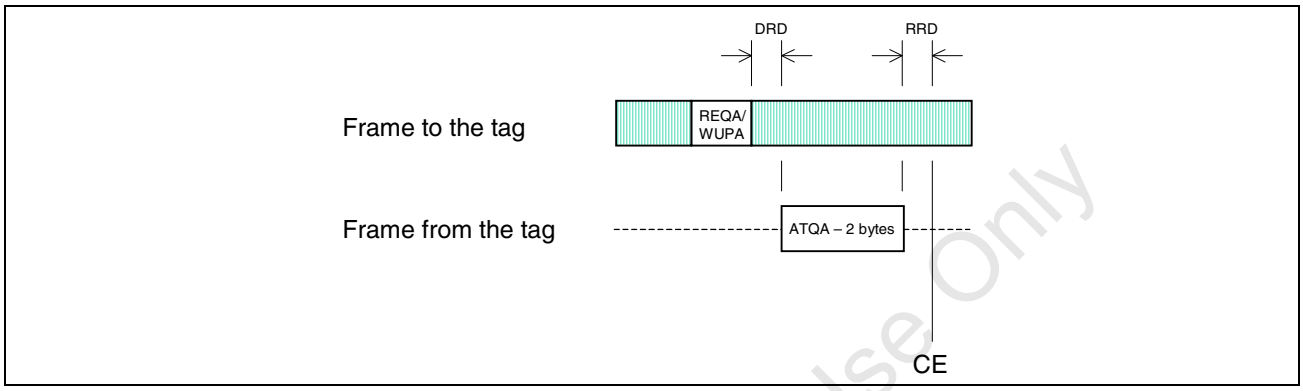


Figure 8: REQA/WUPA and ATQA Command/Response Diagram

The ATQA response bits are as follows:

Table 15: ATQA Response

msb															lsb
b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1
RFU				Proprietary Coding				UID size bit frame		RFU	Bit frame anticollision				
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0				C				0			0				

The ATQA = 0C00h for the BCM20203T512-based tag indicates to the reader/writer that Broadcom-proprietary commands and frames are required.

None of bits b1–5 are set to 1, which indicates to the reader/writer that no bit-frame anticollision is to be used, as referenced in section 6.4.2.1 of ISO/IEC 14443-3:2001(E).

Read Identification (RID)

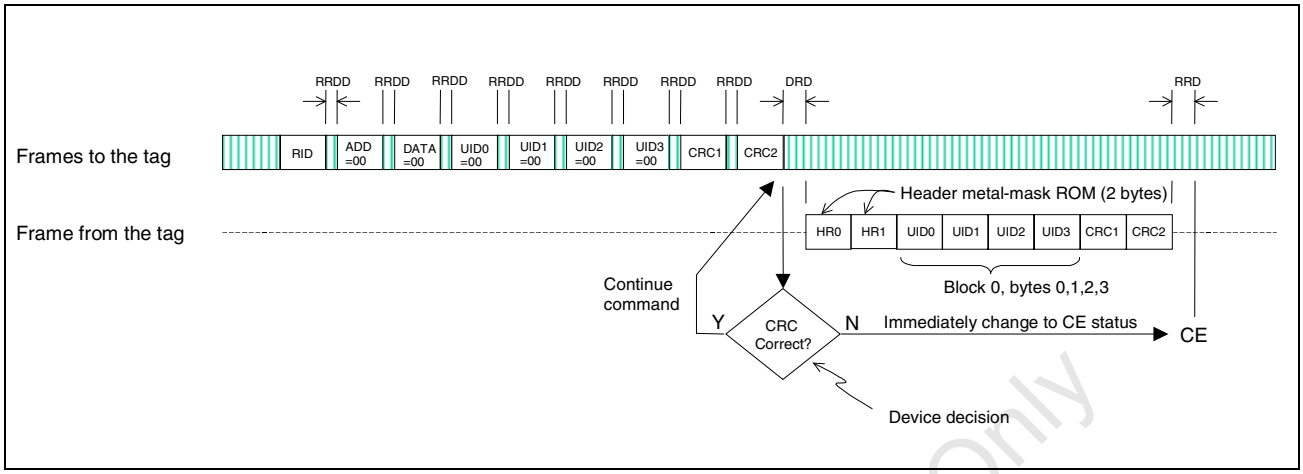


Figure 9: RID Command/Response Diagram

The Read Identification (RID) command, reads the metal-mask header bytes and the four least significant UID bytes from block-0.

The Command frame, then Address frame, Data-byte frame, UID-echo frames, and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag. However, the Address, Data and UID-echo bytes shall be set to zero.

If the CRC is valid, then the HR0 and HR1 bytes, followed by the UID-0, UID-1, UID-2, UID-3, and the frame CRC bytes, will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Read All Blocks 0-E_h (RALL)

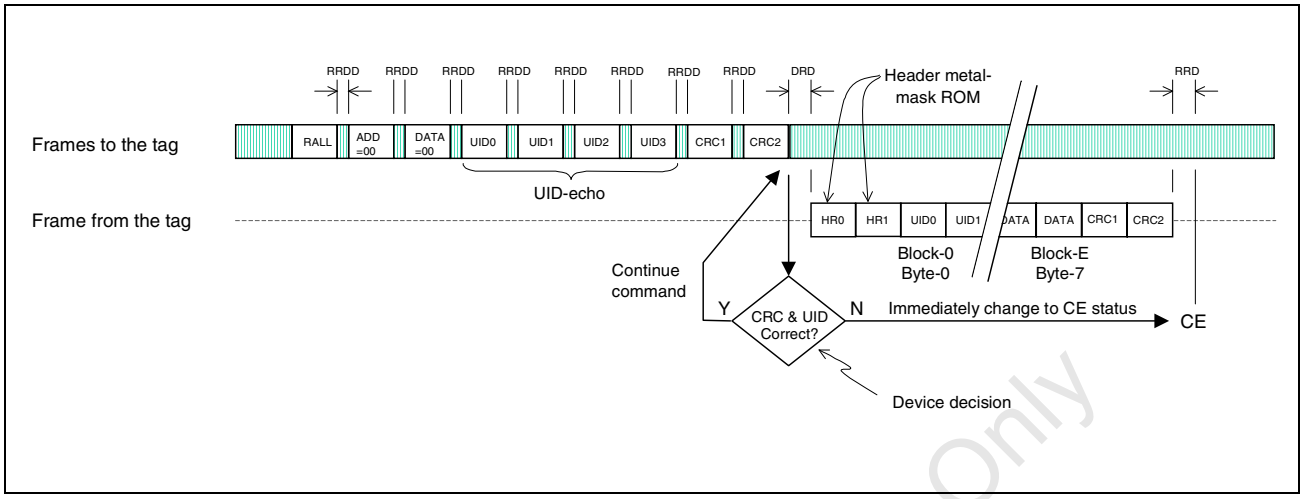


Figure 10: RALL Command/Response Diagram

The RALL command reads-out the two Header ROM bytes followed by the whole of the memory blocks 0-E_h.

The Command frame, then Address frame, Data-byte frame, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag. However, the Address and Data-bytes shall be set to zero.

If the UID and CRC are valid, the HR0 and HR1 bytes, followed by the contents of memory blocks 0-E_h and the frame CRC bytes, will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Read Byte (READ)

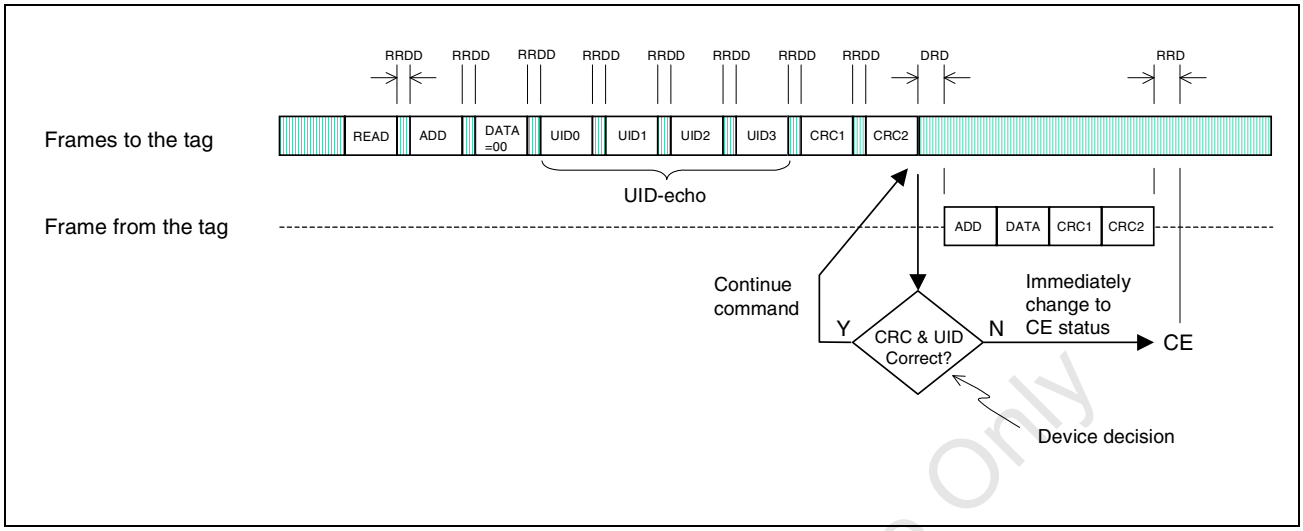


Figure 11: READ Command/Response Diagram

The READ command relates to a single EEPROM memory byte within blocks 0-E_h. The byte address, (Block number and byte number), as defined in Table 10 on page 23, shall be sent with the command.

The Command frame, then Address frame, Data-byte frame, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag. However, the Data-byte shall be set to zero.

If the CRC and UID are valid, the requested memory data byte is read from memory. The Address, followed by the read data byte and the frame CRC bytes will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Write-Erase Byte (WRITE-E)

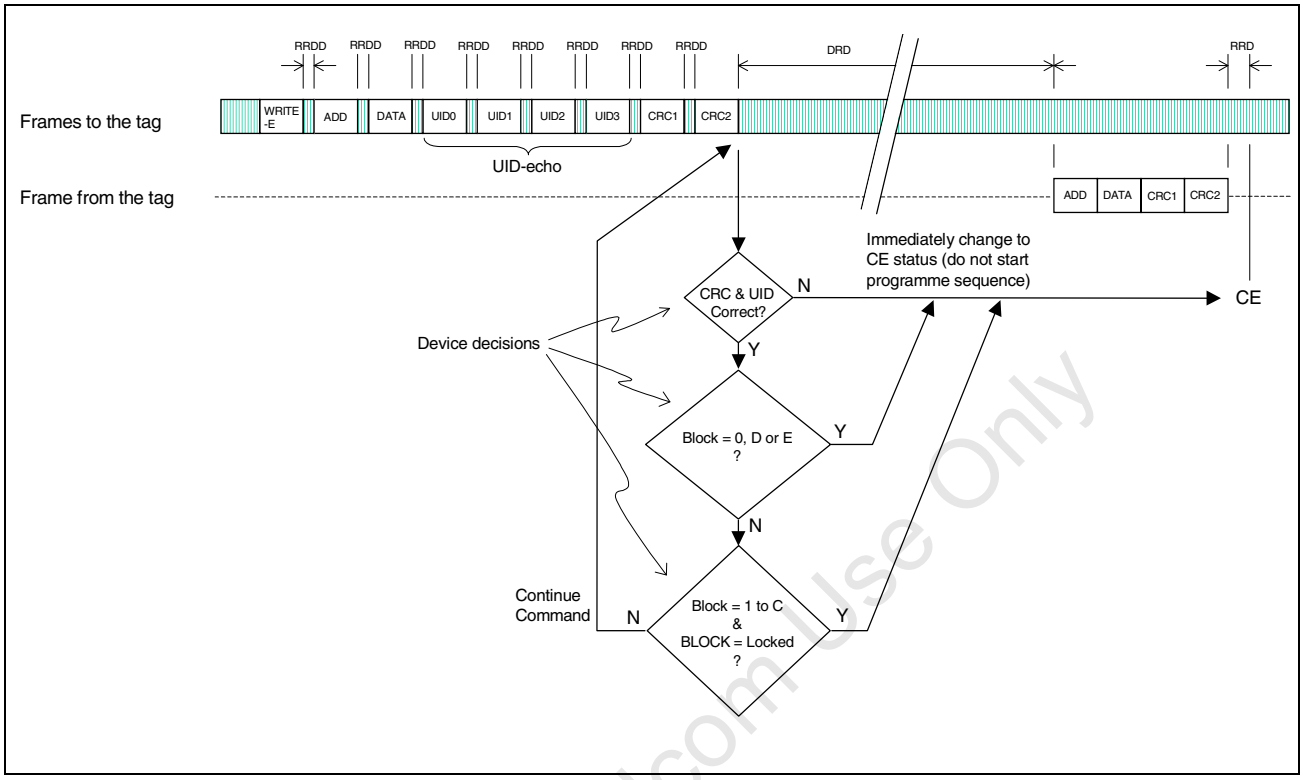


Figure 12: WRITE-E Command/Response Diagram

The WRITE-E (Write–Erase) command relates to an individual memory byte within blocks 0-E_h. The target byte address (Block number and byte number), as defined in Table 10 on page 23, shall be sent with the command. This command performs the normal erase-write cycle, (i.e., it erases the target byte before it writes the new data).

If any of Block-0 to Block-D is locked, then WRITE-E is barred from those blocks. Additionally, WRITE-E is always barred from Blocks 0, D, or E because these are automatically in the locked condition.

The Command frame, then Address frame, Data-byte frame, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag.

If the UID and CRC are valid, (and WRITE-E is not barred), the EE memory erase-write cycle is carried out. The byte is then read back from the EE memory. The address, followed by the data byte and the frame CRC bytes are then sent back to the reader/writer.

If WRITE-E is barred, the erase-write cycle is skipped — no write operation occurs — and without waiting the program-time, the BCM20203T512 tag will enter Ready status, waiting for a new command.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Write-No-Erase Byte (WRITE-NE)

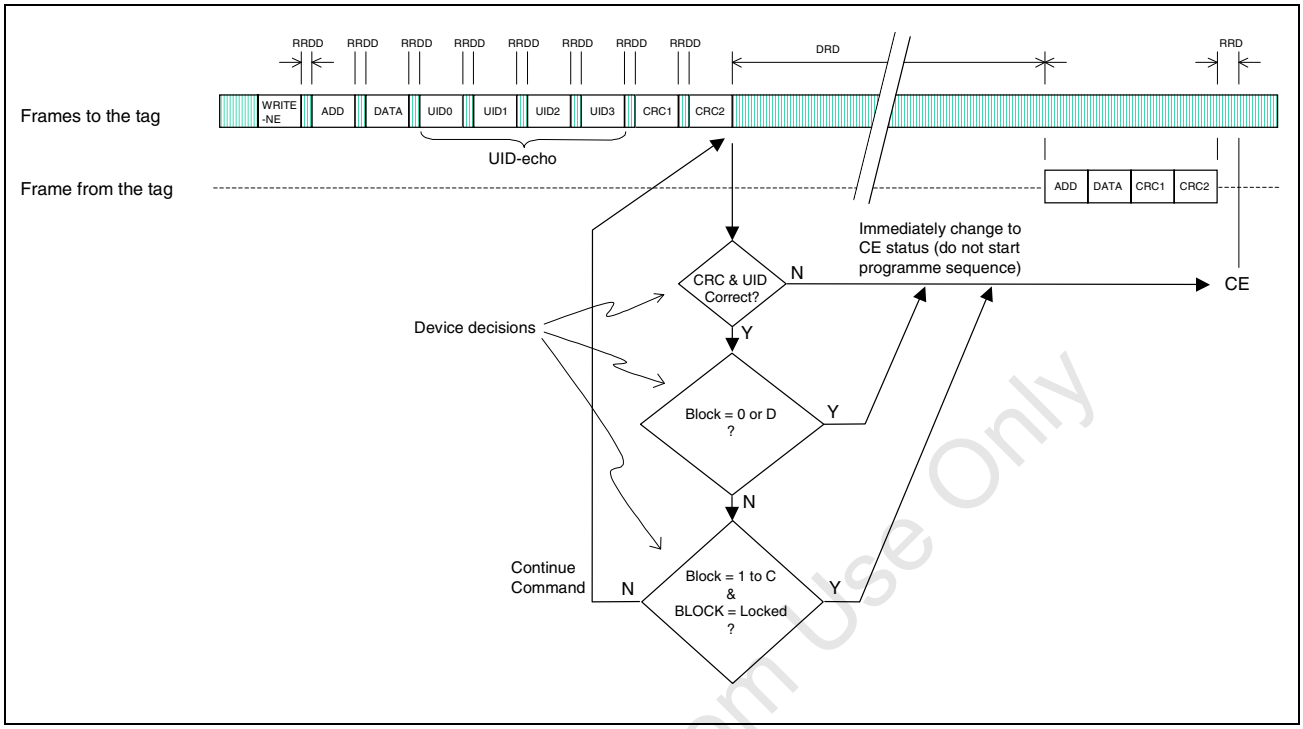


Figure 13: WRITE-NE Command/Response Diagram

The WRITE-NE (Write-No-Erase) command relates to an individual memory byte within blocks 0-E_h. The target byte address (Block number and byte number), as defined in Table 10 on page 23, shall be sent with the command. This command does not erase the target byte before writing the new data, and the execution time is approximately half that of the normal write command (WRITE-E). Bits can be set, but not reset (i.e., data bits previously set to a 1 cannot be reset to a 0).

The WRITE-NE command is available for three main purposes:

- Lock — to set the lock bit for a block.
- OTP — to set OTP bits (bytes 2–7 of Block-E), where between 1- and 8-OTP bits can be set with a single WRITE-NE command.
- A fast-write in order to reduce overall time to write data to memory blocks for the first time given that the original condition of memory is zero.

If any of Block-1 to Block-C is locked, then WRITE-E is barred from that block.

WRITE-NE is not barred from Block-E to allow setting of lock and OTP bits.

The Command frame, then Address frame, Data-byte frame, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag.

If the UID and CRC are valid, (and WRITE-NE is not barred), the EE memory write-no-erase cycle is carried out. The byte is then read back from the EE memory. The Address, followed by the Data byte, and the frame CRC bytes are then sent back to the reader/writer.

If WRITE-NE is barred, the write-no-erase cycle is skipped — no write operation occurs — and without waiting the program-time, the BCM20203T512 tag will return to the Ready state and wait for a new command.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Read Segment (RSEG)

The RSEG command reads-out a complete segment of memory. A segment consists of 16 blocks, i.e., 128-bytes of memory.

The command frames to the BCM20203T512 tag are similar to the RALL command with the ADD replaced by ADDS (Address Segment) to select the required segment with the format as defined in Table 11 on page 23.

The Command-Response summary is given in Table 7 and Table 8 on page 21.

The Command frame, then Address frame, eight data-byte frames, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer to the BCM20203T512 tag. However, the eight data-bytes SHALL be set to zero.

If the UID and CRC are valid, then the ADDS, followed by the 128-byte contents of that segment, and the frame CRC bytes will be sent back to the NFC-Forum device in NFC Forum reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Read 8 Bytes (READ8)

The READ8 command reads-out a block of memory.

The command frames to the BCM20203T512 tag are similar to the single byte READ command with the ADD replaced by ADD8 (Address 8) to select the required block with the format as defined in Table 12 on page 23.

The Command-Response summary is given in Table 7 and Table 8 on page 21.

The Command frame, then Address frame, eight data-byte frames, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the NFC Forum device in NFC Forum reader/writer mode to the BCM20203T512 tag. However, the eight data-bytes shall be set to zero.

If the UID and CRC are valid, then the ADD8, followed by the 8 data-bytes contents read from that block, and the frame CRC bytes will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Write-Erase 8 Bytes (WRITE-E8)

The WRITE-E8 command writes with erase to a block of memory.

The command frames to the BCM20203T512 tag are similar to the single-byte WRITE-E command with the ADD replaced by ADD8 (Address 8) to select the required block with the format as defined in Table 12 on page 23.

The Command-Response summary is given in Table 7 and Table 8 on page 21.

The Command frame, then Address frame, eight data-byte frames for the data to be written, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer.

If the UID and CRC are valid, then the ADD8, followed by the 8 data-bytes contents just written to that block, and the frame CRC bytes will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Write-No-Erase 8 Bytes (WRITE-NE8)

The WRITE-E8 command writes with no erase to a block of memory.

The command frames to the BCM20203T512 tag are similar to the single-byte WRITE-NE command with the ADD replaced by ADD8 (Address 8) to select the required block with the format as defined in Table 12 on page 23.

The Command-Response summary is given in Table 7 and Table 8 on page 21.

The Command frame, then Address frame, eight data-byte frames for the data to be written, UID-echo frames (with UID data received from previous RID command), and CRC frames shall be sent by the reader/writer mode to the BCM20203T512 tag.

If the UID and CRC are valid, then the ADD8, followed by the 8 data-bytes contents just written to that block, and the frame CRC bytes will be sent back to the reader/writer.

As a precondition, this command requires that the BCM20203T512 tag be in the Ready state and afterwards the BCM20203T512 tag remains in Ready state.

Lock Control/Status Bits

All memory blocks are separately lockable.

When a block's lock-bit is set to a 1_b, it cannot be changed back to 0_b again, and that block becomes irreversibly frozen as read-only.

The lock-bits are stored in the Block-E_h and Block-F_h, and they operate in a bit-wise OTP fashion.

The WRITE-NE command with appropriate data pattern should be used by the reader/writer to set individual lock-bits. A single WRITE-NE command can be used to set between one and eight lock-bits.

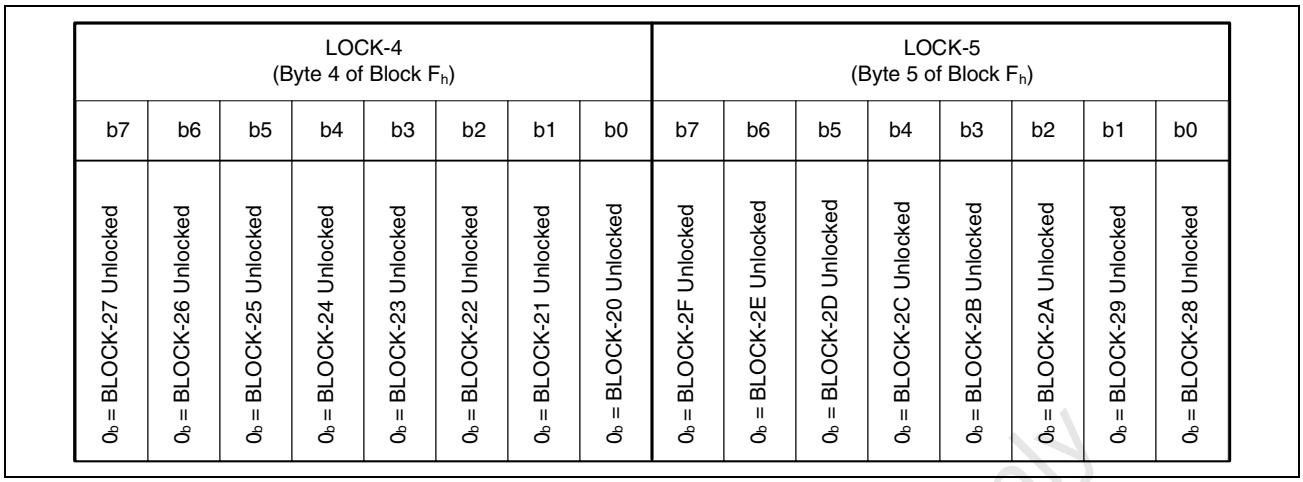
Figure 14, Figure 15, Figure 16 and Figure 17 show the factory default settings.

LOCK-0 (Byte 0 of Block E_h)								LOCK-1 (Byte 1 of Block E_h)							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0_b = BLOCK-07 Unlocked	0_b = BLOCK-06 Unlocked	0_b = BLOCK-05 Unlocked	0_b = BLOCK-04 Unlocked	0_b = BLOCK-03 Unlocked	0_b = BLOCK-02 Unlocked	0_b = BLOCK-01 Unlocked	1_b = BLOCK-00 Locked	1_b = BLOCK-0F Locked	1_b = BLOCK-0E Locked	1_b = BLOCK-0D Locked	0_b = BLOCK-0C Unlocked	0_b = BLOCK-0B Unlocked	0_b = BLOCK-0A Unlocked	0_b = BLOCK-09 Unlocked	0_b = BLOCK-08 Unlocked

Figure 14: LOCK-0 and LOCK-1

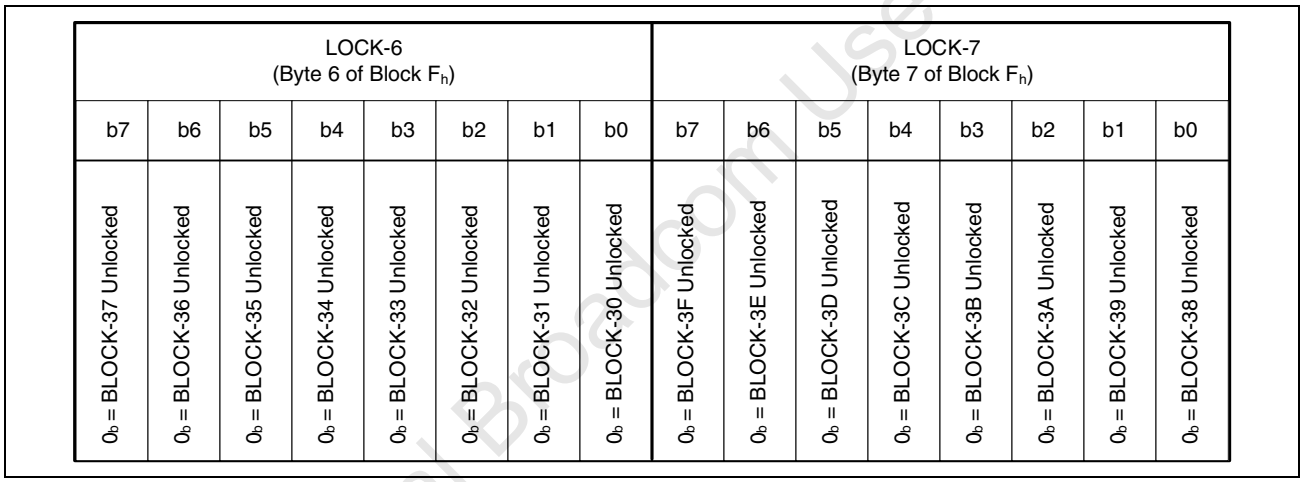
LOCK-2 (Byte 2 of Block F_h)								LOCK-3 (Byte 3 of Block F_h)							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0_b = BLOCK-17 Unlocked	0_b = BLOCK-16 Unlocked	0_b = BLOCK-15 Unlocked	0_b = BLOCK-14 Unlocked	0_b = BLOCK-13 Unlocked	0_b = BLOCK-12 Unlocked	0_b = BLOCK-11 Unlocked	0_b = BLOCK-10 Unlocked	0_b = BLOCK-1F Unlocked	0_b = BLOCK-1E Unlocked	0_b = BLOCK-1D Unlocked	0_b = BLOCK-1C Unlocked	0_b = BLOCK-1B Unlocked	0_b = BLOCK-1A Unlocked	0_b = BLOCK-19 Unlocked	0_b = BLOCK-18 Unlocked

Figure 15: LOCK-2 and LOCK-3



LOCK-4 (Byte 4 of Block F_h)								LOCK-5 (Byte 5 of Block F_h)							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0_b = BLOCK-27 Unlocked	0_b = BLOCK-26 Unlocked	0_b = BLOCK-25 Unlocked	0_b = BLOCK-24 Unlocked	0_b = BLOCK-23 Unlocked	0_b = BLOCK-22 Unlocked	0_b = BLOCK-21 Unlocked	0_b = BLOCK-20 Unlocked	0_b = BLOCK-2F Unlocked	0_b = BLOCK-2E Unlocked	0_b = BLOCK-2D Unlocked	0_b = BLOCK-2C Unlocked	0_b = BLOCK-2B Unlocked	0_b = BLOCK-2A Unlocked	0_b = BLOCK-29 Unlocked	0_b = BLOCK-28 Unlocked

Figure 16: LOCK-4 and LOCK-5



LOCK-6 (Byte 6 of Block F_h)								LOCK-7 (Byte 7 of Block F_h)							
b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
0_b = BLOCK-37 Unlocked	0_b = BLOCK-36 Unlocked	0_b = BLOCK-35 Unlocked	0_b = BLOCK-34 Unlocked	0_b = BLOCK-33 Unlocked	0_b = BLOCK-32 Unlocked	0_b = BLOCK-31 Unlocked	0_b = BLOCK-30 Unlocked	0_b = BLOCK-3F Unlocked	0_b = BLOCK-3E Unlocked	0_b = BLOCK-3D Unlocked	0_b = BLOCK-3C Unlocked	0_b = BLOCK-3B Unlocked	0_b = BLOCK-3A Unlocked	0_b = BLOCK-39 Unlocked	0_b = BLOCK-38 Unlocked

Figure 17: LOCK-6 and LOCK-7

UID Format

The 7-byte Unique Identification (UID), number is locked into block 00. See Table 1 on page 13.

Byte 7 is reserved for future use and should be ignored. Byte 6 (UID-6) is the manufacturer's identification, and is equal to 25_h.

Section 6: Wafer and Die Information

Overview

This section describes the properties and the requirements for storing the BCM20203T512 wafer that has been diced and supplied on non-UV tape rings. The BCM20203T512 is also available as a DFN packaged IC. For more information, see Section 7: “Mechanical Information,” on page 40.

Base Wafer Properties

Table 16: Base Wafer Properties

Property	*Value*
Test	Wafers are supplied tested with wafer map
Wafer material	Silicon
Doping	Boron
Wafer diameter	8 inches supplied as a whole in diced form on a tape ring
Carriage method from Test/Foundry	Each wafer mounted on a metal ring, up to 25 per cassette
Back-side metallization	None
Pad material	Aluminum

Recommended Storage Conditions

A temperature, humidity, and contamination-controlled environment is required to maintain the wafer quality.

Table 17: Recommended Storage Conditions

Parameter	*Value*	*Units*
Temperature	65 to 75	°F
Humidity	<30	%
Nitrogen (N_2)	Dryness < 4 (~–114°C dew point)	ppm
Particle count	Class 1000	–

Broadcom recommends that bond pads on wafers in storage be inspected on a regular basis for signs of oxidation. Where oxidation is present, plasma cleaning is recommended prior to assembly. However, do not perform plasma cleaning while the die is on the blue film/tape or in waffle packs.

Expected Usable Life

Broadcom recommends that the dies be removed from the wafer within 3 months of processing because the adhesive strength of the dicing tape increases with time. If you expect that the dies need to be stored longer than 3 months, then the dies should be removed from the wafer and placed in a waffle pack.

Note: It is important that the recommended storage conditions in Table 17 are followed or the adhesive of the ring may become too strong and make the removal of the dies difficult.

Wafer Physical Data

The BCM20203T512 is a nickel-gold bumped IC. See Figure 18 on page 38 for the wafer dimensions.

The BCM20203T512 is supplied as bumped, ground, and sawn wafers on film.

Table 18: Wafer Physical Data

Parameter	*Value*	*Units*
Die size (including guard ring)	0.59 x 0.59	mm
Wafer background nominal thickness	150	µm
L1, L2 bond pad passivation opening	≥ 80	µm
Operating temperature range	–25 to +50	°C
Non-operational data retention (i.e., storage temperature) range	–40 to +70	°C

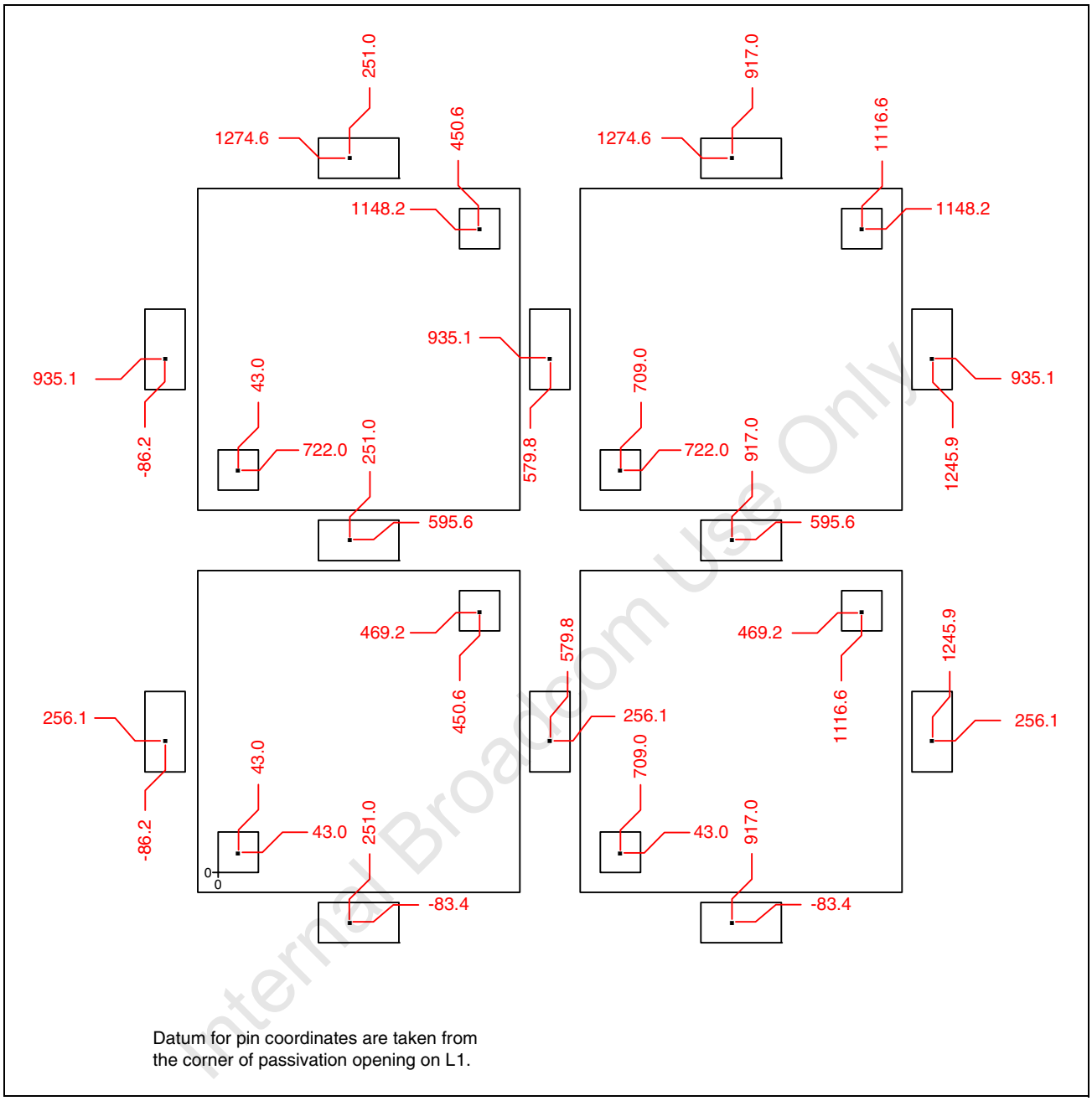
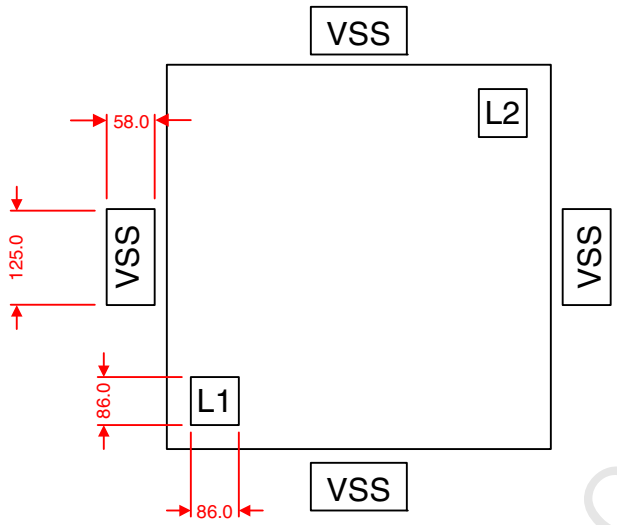


Figure 18: Die Size and Wafer Step Dimensions



Pad dimensions are for passivation openings.

Figure 19: Pad Layout

Section 7: Mechanical Information

Figure 20 shows the DFN package information for the BCM20203A0KMLG.

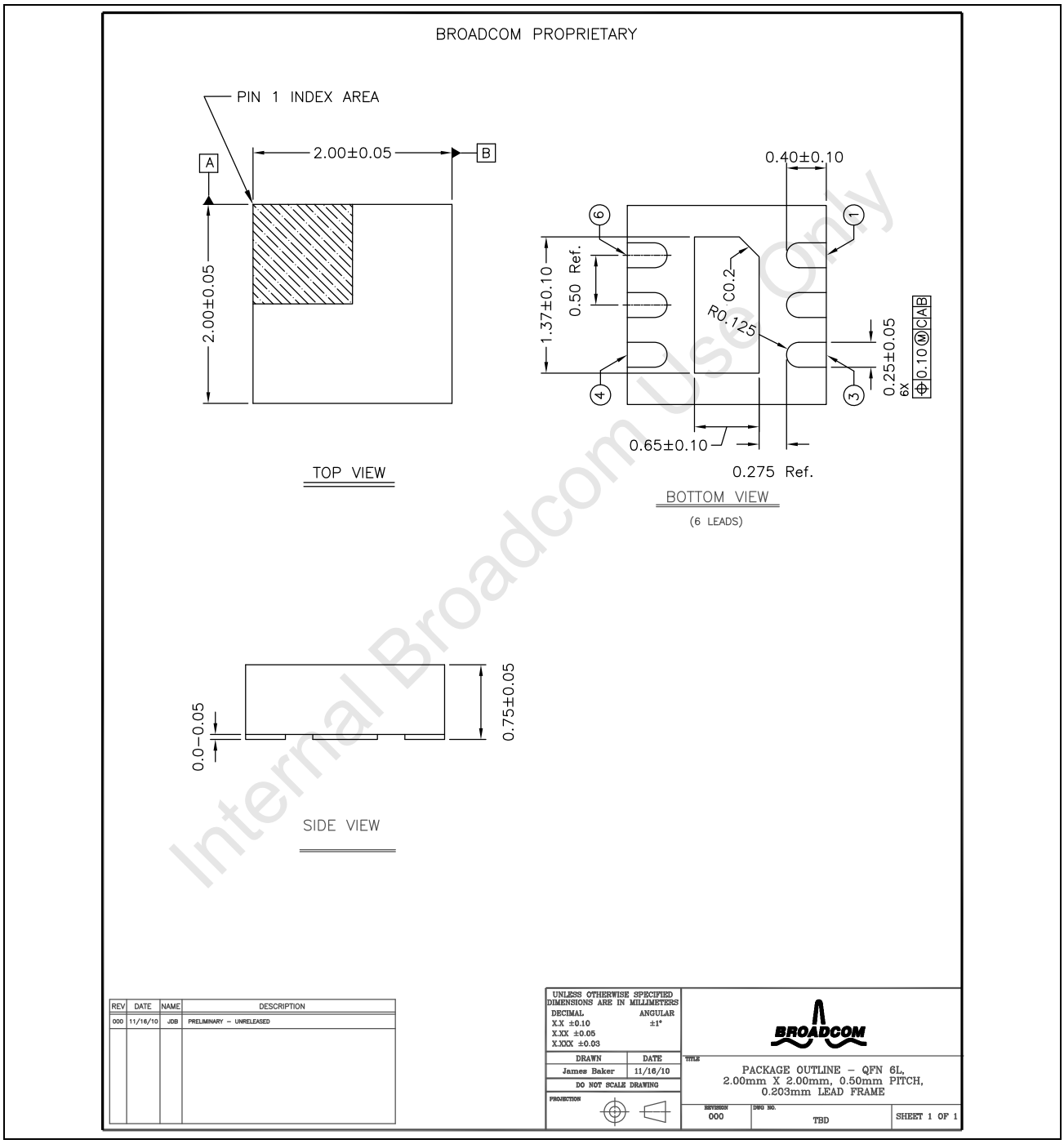


Figure 20: 2.00 X 2.00 mm, 0.50 mm Pitch, 6-lead DFN Package

Section 8: Ordering Information

Table 19: Ordering Information

Part Number	*Description*
BCM20203T512	0.59 x 0.59 mm die
BCM20203A0KMLG	2.00 X 2.00 mm, 0.50 mm pitch, 6-lead DFN on tape and reel

Note: Die are supplied as bumped, ground, and sawn wafers on film with accompanying test wafer map. Contact your Broadcom Sales representative for MOQ and for advice on the number of wafers required to achieve the known good number of die.

Appendix A: NFC Forum 'Initialized State'

Memory Contents

Table 20 through Table 23 on page 45 show EEPROM memory maps, Segment0 through Segment3, respectively.

Table 20: EEPROM Memory Map (Segment0)

Type	*Block Number*	*Byte 0 (LSB)*	*Byte 1*	*Byte 2*	*Byte 3*	*Byte 4*	*Byte 5*	*Byte 6*	*Byte 7 (MSB)*	*Lockable*
UID	00	UID-0	UID-1	UID-2	UID-3	UID-4	UID-5	25_h	–	Locked
Data	01	CC0 (NMN) E1h	CC1 (VNo) 10h	CC2 (TMS) 3Fh	CC3 (RWA) 00h	Lock Control TLV T=01h	Lock Control TLV L=03h	Lock Control TLV V0=F2h	Lock Control TLV V1=30h	Yes
Data	02	Lock Control TLV V2=33h	Memory Control TLV T=02h	Memory Control TLV L=03h	Memory Control TLV V0=F0h	Memory Control TLV V1=02h	Memory Control TLV V2=03h	NDEF Message TLV T=03h	NDEF Message TLV L=00h	Yes
Data	03	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	04	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	05	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	06	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	07	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	08	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	09	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	0A	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	0B	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Data	0C	00h	00h	00h	00h	00h	00h	00h	00h	Yes
Reserved	0D	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	N/A
Lock/OTP	0E	LOCK-0 01h	LOCK-1 E0h	OTP-0 00h	OTP-1 00h	OTP-2 00h	OTP-3 00h	OTP-4 00h	OTP-5 00h	N/A
Lock/OTP	0F	OTP-6 00h	OTP-7 00h	LOCK-2 00h	LOCK-3 00h	LOCK-4 00h	LOCK-5 00h	LOCK-6 00h	LOCK-7 00h	N/A

Table 21: EEPROM Memory Map (Segment1)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	10	–	–	–	–	–	–	–	–	Yes
Data	11	–	–	–	–	–	–	–	–	Yes
Data	12	–	–	–	–	–	–	–	–	Yes
Data	13	–	–	–	–	–	–	–	–	Yes
Data	14	–	–	–	–	–	–	–	–	Yes
Data	15	–	–	–	–	–	–	–	–	Yes
Data	16	–	–	–	–	–	–	–	–	Yes
Data	17	–	–	–	–	–	–	–	–	Yes
Data	18	–	–	–	–	–	–	–	–	Yes
Data	19	–	–	–	–	–	–	–	–	Yes
Data	1A	–	–	–	–	–	–	–	–	Yes
Data	1B	–	–	–	–	–	–	–	–	Yes
Data	1C	–	–	–	–	–	–	–	–	Yes
Data	1D	–	–	–	–	–	–	–	–	Yes
Data	1E	–	–	–	–	–	–	–	–	Yes
Data	1F	–	–	–	–	–	–	–	–	Yes

Table 22: EEPROM Memory Map (Segment2)

Type	Block Number	Byte 0 (LSB)	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7 (MSB)	Lockable
Data	20	–	–	–	–	–	–	–	–	Yes
Data	21	–	–	–	–	–	–	–	–	Yes
Data	22	–	–	–	–	–	–	–	–	Yes
Data	23	–	–	–	–	–	–	–	–	Yes
Data	24	–	–	–	–	–	–	–	–	Yes
Data	25	–	–	–	–	–	–	–	–	Yes
Data	26	–	–	–	–	–	–	–	–	Yes
Data	27	–	–	–	–	–	–	–	–	Yes
Data	28	–	–	–	–	–	–	–	–	Yes
Data	29	–	–	–	–	–	–	–	–	Yes
Data	2A	–	–	–	–	–	–	–	–	Yes
Data	2B	–	–	–	–	–	–	–	–	Yes
Data	2C	–	–	–	–	–	–	–	–	Yes
Data	2D	–	–	–	–	–	–	–	–	Yes
Data	2E	–	–	–	–	–	–	–	–	Yes
Data	2F	–	–	–	–	–	–	–	–	Yes

Table 23: EEPROM Memory Map (Segment3)

Type	*Block Number*	*Byte 0 (LSB)*	*Byte 1*	*Byte 2*	*Byte 3*	*Byte 4*	*Byte 5*	*Byte 6*	*Byte 7 (MSB)*	*Lockable*
Data	30	–	–	–	–	–	–	–	–	Yes
Data	31	–	–	–	–	–	–	–	–	Yes
Data	32	–	–	–	–	–	–	–	–	Yes
Data	33	–	–	–	–	–	–	–	–	Yes
Data	34	–	–	–	–	–	–	–	–	Yes
Data	35	–	–	–	–	–	–	–	–	Yes
Data	36	–	–	–	–	–	–	–	–	Yes
Data	37	–	–	–	–	–	–	–	–	Yes
Data	38	–	–	–	–	–	–	–	–	Yes
Data	39	–	–	–	–	–	–	–	–	Yes
Data	3A	–	–	–	–	–	–	–	–	Yes
Data	3B	–	–	–	–	–	–	–	–	Yes
Data	3C	–	–	–	–	–	–	–	–	Yes
Data	3D	–	–	–	–	–	–	–	–	Yes
Data	3E	–	–	–	–	–	–	–	–	Yes
Data	3F	–	–	–	–	–	–	–	–	Yes

Explanation

When a BCM20203T512-based tag is in the Initialized state, the main memory area is set as follows:

- Lock-0 = 01_h, Lock-1 = $E0_h$, Lock-2 = Lock-3 = Lock-4 = Lock-5 = Lock-6 = 00_h
- The CC is set as follows:
  - CC0 = $E1_h$ the NDEF magic number.
  - CC1 = 10_h to indicate support of the version 1.0 (major number 1_h, minor number 0h) of the NFC Forum Type 1 Tag Operation Specification.
  - CC2 = $3F_h$ (n=63, 8*(n+1) = 512 of physical memory size).
  - CC3 = 00_h to indicated read and write access granted without any security.
- The data area contains the following TLVs:
  - Lock Control TLV: T = 01_h, L = 03_h, V0 = $F2_h$, V1 = 30_h, V2 = 33_h

    Indicates that each lock bit locks 1 page, each page is 8 bytes, and the lock area is 48 bits long, starting at the byte address 122 as calculated by the formula:

    ByteAddr = PageAddr*$2^{BytesPerPage}$ + ByteOffset = 15 * 2^3 + 2 = 122 where:
    - Position = $F2_h$ means PageAddr = F_h = 15 and ByteOffset = 2
    - Size = 30_h = 6*8 = 48 bits
    - PageControl = 33_h means BytesPerPage = 3h (2^3 = 8 bytes) and BytesLockedPerLockBit = 3h (2^3 = 8 bytes).
  - Reserved Memory Control TLV: T = 02_h, L = 03_h, V0 = $F0_h$, V1 = 02_h, V2 = 03_h

    Indicates that the reserved area is 2 bytes long starting at the byte address 120 as calculated by the formula:

    ByteAddr = PageAddr*$2^{BytesPerPage}$ + ByteOffset = 15 * 2^3 + 0 = 120 where:
    - Position = $F0_h$ contains PageAddr = F_h = 15 and ByteOffset = 0
    - Size = 02_h = 2 bytes
    - PageControl = 03h contains BytesPerPage = 3h as the least significant nibble. Most significant nibble is ignored.

Appendix B: Hints and Tips

Purpose

This section is intended to clarify the communication protocol and CRC calculation.

The following is an important clarification of the BCM20203T512 command set.

- Commands sent to a BCM20203T512 tag (apart from the REQA or WUPA) all consist of 7 bytes followed by a 2-byte checksum.
- Each byte is sent within its own frame.
- A frame start-of-message sequence proceeds each byte and a frame end-of-message sequence follows each byte.

REQA Response

The BCM20203T512 ATQA response to a REQA or WUPA command consists of byte 0x00 followed by byte 0x0C.

Some RFID documentation specifies the REQA response as a 16-bit value, where the least significant byte is transmitted before the most significant byte. For example, the 16-bit representation of the BCM20203T512 ATQA response in this format is 0x0C00 (where 0x00 is transmitted first and 0x0C second).

Communication Example

Table 24 illustrates reading and writing to a BCM20203T512 tag with UID = 00,00,00,00,00,00,00,00 and all memory initialized to zero. HR1 = 48 for this example.

Bytes are transmitted with the least significant bit first. For example, Table 24 shows that REQA (0x26, binary 010 0110) is transmitted as logic 0, logic 1, logic 1, logic 0, logic 0, logic 1, and finally logic 0.

In each column, the left-most byte (bit) is transmitted first and the right-most byte (bit) transmitted last. **S** refers to frame start and **E** to frame end sequences. The bit sequences are shown in brackets and include the odd parity bit.

Table 24: BCM20203T512 Communication Examples (UID = 00,00,00,00)

Description	*Command to BCM20203T512 (Hex)*	*Response from BCM20203T512 (Hex)*
REQA	26 (S 0110010 E)	00,0C (S 00000000 1 00110000 1 E)
RID	78,00,00,00,00,00,00,D0,43 (S 0001111 E S 00000000 E …)	11,48,00,00,00,00,16,2A
RALL	00,00,00,00,00,00,00,70,8C	11,48,<120 zero bytes>,C5,2D (total 124 bytes)
READ	01,08,00,00,00,00,00,FD,32	08,00,87,C1
WRITE_E	53,08,12,00,00,00,00,41,D5	08,12,14,F2
READ	01,08,00,00,00,00,00,FD,32	08,12,14,F2
RALL	00,00,00,00,00,00,00,70,8C	11,48,00,00,00,00,00,00,00,12,<111 zero bytes>,62,07 (total 124 bytes)

Communication Summary

Commands sent to BCM20203T512 tag have the following format:

- First byte is 7 bits
- Remaining bytes are 8 bits
- Least significant bit is sent first
- There are no parity bits
- A frame-start sequence proceeds each byte (including the CRC bytes) and a frame-end follows each byte
- The CRC_B is appended to all commands apart from REQA and WUPA

Responses from the BCM20203T512 tag have the following format:

- All bytes are 8 bits
- Least significant bit is sent first
- A parity bit (odd) follows each byte
- A response begins with a start-frame sequence, and ends with a stop-frame sequence. The response bytes (including CRC) are between these sequences.
- The CRC_B is appended to all responses apart from ATQA

CRC Clarification

- The CRC is CRC_B as specified by ISO/IEC 14443-3:2001(E) Annex B.
- The CRC is always calculated on 8-bit bytes.
- Although the first BCM20203T512 command byte is transmitted as 7-bits, 8-bits must still be used to calculate the CRC (i.e., the 7 bits of the command must be padded with a zero in the MSB).
- The CRC is calculated on all data bytes, excluding the start, end, parity, and CRC bits.
- The 16-bit CRC is transmitted with the least significant byte first, then the most significant byte.

Code Sample Written in C for CRC Calculation

```
© ISO/IEC 2000 – All rights reserved (Extracted from ISO/IEC 14443-3)
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define CRC_A 1
#define CRC_B 2
#define BYTE unsigned char

unsigned short UpdateCrc(unsigned char ch, unsigned short *lpwCrc)
{
ch = (ch^(unsigned char)((*lpwCrc) & 0x00FF));
ch = (ch^(ch<<4));
*lpwCrc = (*lpwCrc >> 8)^((unsigned short)ch << 8)^((unsigned short)ch<<3)^((unsigned short)ch>>4);
return(*lpwCrc);
}

void ComputeCrc(int CRCType, char *Data, int Length,
BYTE *TransmitFirst, BYTE *TransmitSecond)
{
unsigned char chBlock;
unsigned short wCrc;
switch(CRCType) {
case CRC_A:
wCrc = 0x6363; /* ITU-V.41 */
break;
case CRC_B:
wCrc = 0xFFFF; /* ISO/IEC 13239 (formerly ISO/IEC 3309) */
break;
default:
return;
}
do {
chBlock = *Data++;

UpdateCrc(chBlock, &wCrc);
} while (--Length);
if (CRCType == CRC_B)
wCrc = ~wCrc; /* ISO/IEC 13239 (formerly ISO/IEC 3309) */
*TransmitFirst = (BYTE) (wCrc & 0xFF);
*TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
```

```
return;
}

BYTE BuffCRC_A[10] = {0x12, 0x34};
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56};
unsigned short Crc;
BYTE First, Second;
FILE *OutFd;
int i;

int main(void)
{
printf("CRC-16 reference results ISO/IEC 14443-3\n");
printf("Crc-16 G(x) = x^16 + x^12 + x^5 + 1\n\n");
printf("CRC_A of [ ");
for(i=0; i<2; i++) printf("%02X ",BuffCRC_A[i]);
ComputeCrc(CRC_A, BuffCRC_A, 2, &First, &Second);
printf("] Transmitted: %02X then %02X.\n", First, Second);
printf("CRC_B of [ ");
for(i=0; i<4; i++) printf("%02X ",BuffCRC_B[i]);
ComputeCrc(CRC_B, BuffCRC_B, 4, &First, &Second);
printf("] Transmitted: %02X then %02X.\n", First, Second);
return(0);
}
```

Code Sample Written in Perl for CRC Calculation

```
#!/usr/bin/perl
# CRC calculator for Topaz
# original Aug 2003

print "Reader to tag - Enter hex for each Byte, empty string to end\n";
$poly = 0x0810;#polynomial - we xor bits 11 and 4 with in0
$crc  = 0xffff;#initial value
$m="0"; $b=0;

for($b=0; $b<200; $b++) {
    print "Byte $b: ";
    $_=<STDIN>;
    chomp;
    if ($_ eq "") {last;}
    $m = hex($_);   #data Byte
    $v=0x01;    #bit marker - start at LSB of data

    for ($i=0; $i<8; $i++) {
    $crcmsb=($crc & 0x8000)>>15;#MSB of the crc
    $din = ($m & $v)>>$i;#selected data bit
    $in0 = $crcmsb ^ $din;

    if ($in0) {
        $crc = $crc ^ $poly;#xor with polynomial
    }
    $crc = ($crc << 1) & 0xffff;#left shift the crc
    if ($in0) {$crc = $crc+1;}

    $v = $v << 1;#next bit of data
```

```
    }
}
#printf "crc before transformation = %x\n", $crc;
#now invert and reflect

$crc = $crc ^ 0xffff;#invert
$out = 0;      #output value
for ($i=0; $i<16; $i++) {
    $j = 8*int($i/8) + (7-$i%8);#calculate destination bit (reflection)
    $bit = ($crc>>$i) & 1;
    $out = $out + $bit*(2**$j);
}

printf "output CRC = %x\n", $out;
```

Scope Traces Illustrating BCM20203T512 Communication

This section uses oscilloscope traces to illustrate BCM20203T512-based tag communications.

The traces show the following signals:

2: Sniffer coil placed next to the reader antenna

D0: Digital signal showing transmissions from the reader to the BCM20203T512 tag

D2: Digital signal showing transmissions from the BCM20203T512 tag to the reader

The scope traces were taken during a read of 1 byte from BCM20203T512 memory location 0x08 using the commands REQA, RID, and READ. The UID is all zero and the data byte at 0x08 has a value of 0x00.

Trace 1: Entire Communication Sequence

Note that the entire communication sequence takes 7.5 ms.

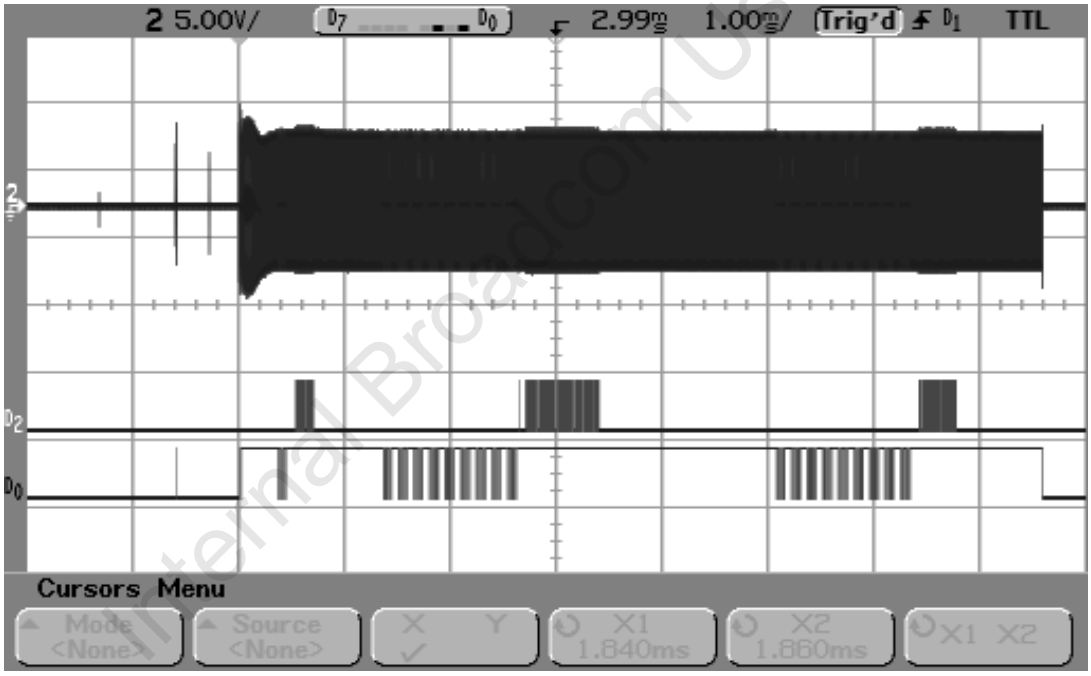


Figure 21: Entire Communication Sequence

Trace 2: Delay from REQA to ATQA Response

Note that the Device Response Delay (DRD) for the REQA command is 86 µs.

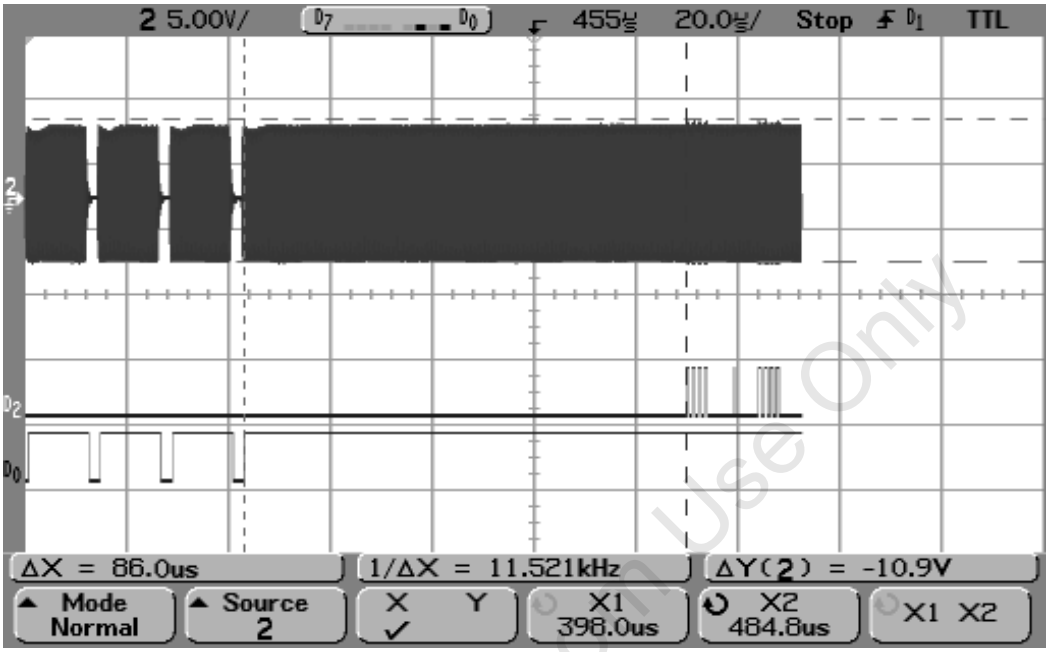


Figure 22: Delay from REQA to ATQA Response

Trace 3: Start of RID Command

Note that the Reader-Reader Data Delay (RRDD) in this example is 65 µs.

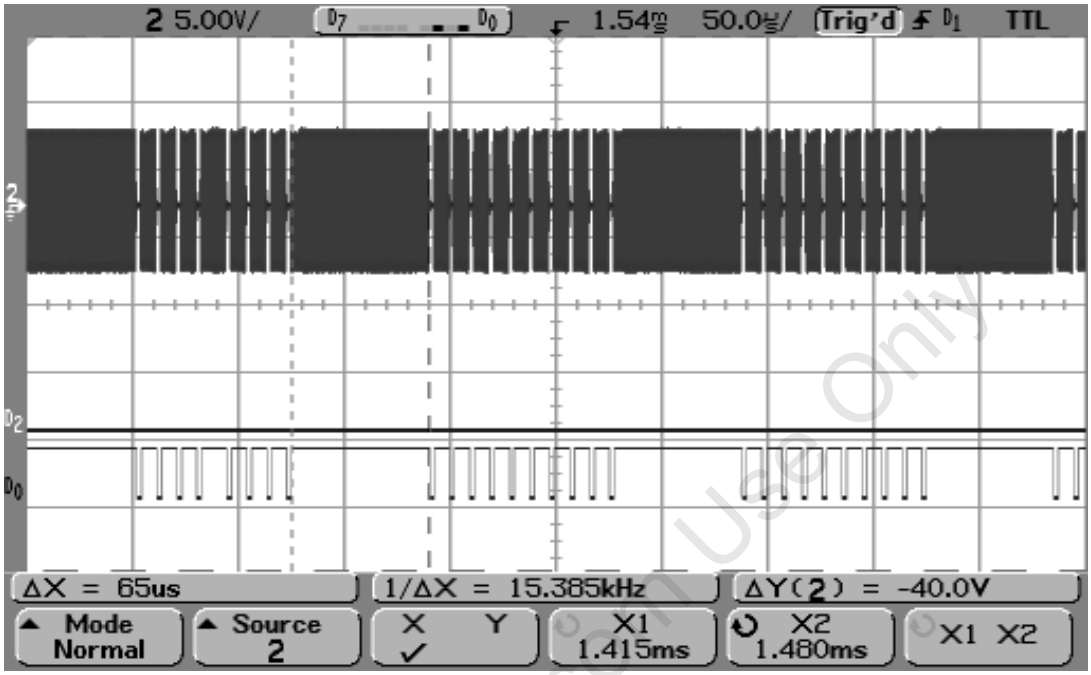


Figure 23: Start of RID Command

Trace 4: End of RID Command

Note that the Device Response Delay (DRD) for the RID command is 86 µs.

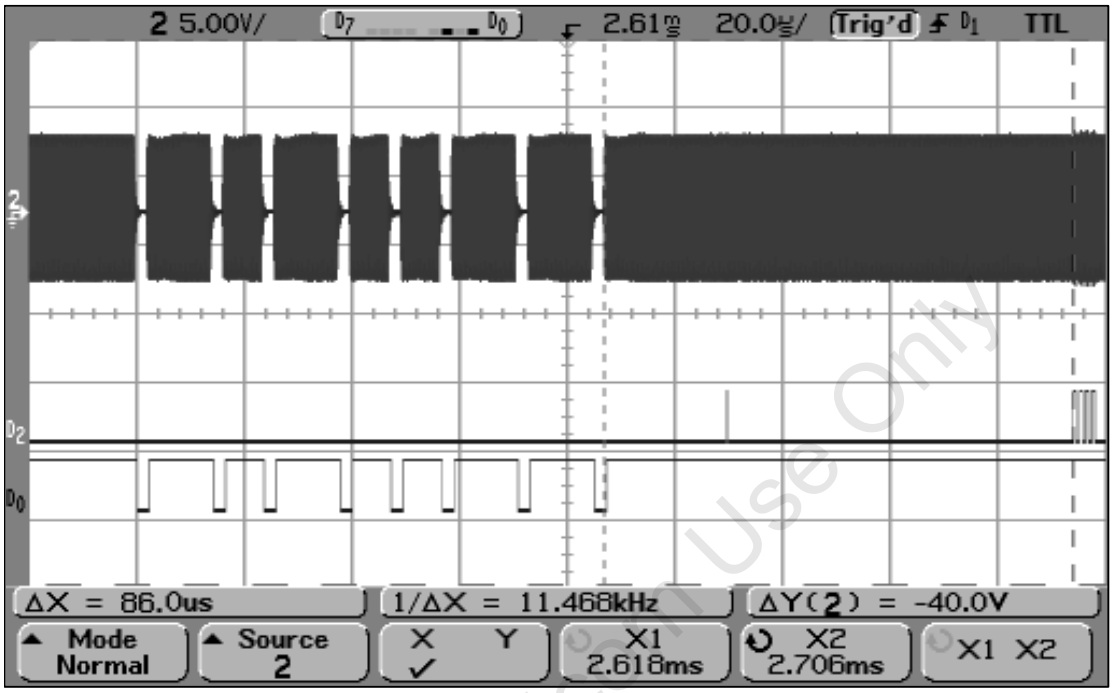


Figure 24: End of RID Command

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